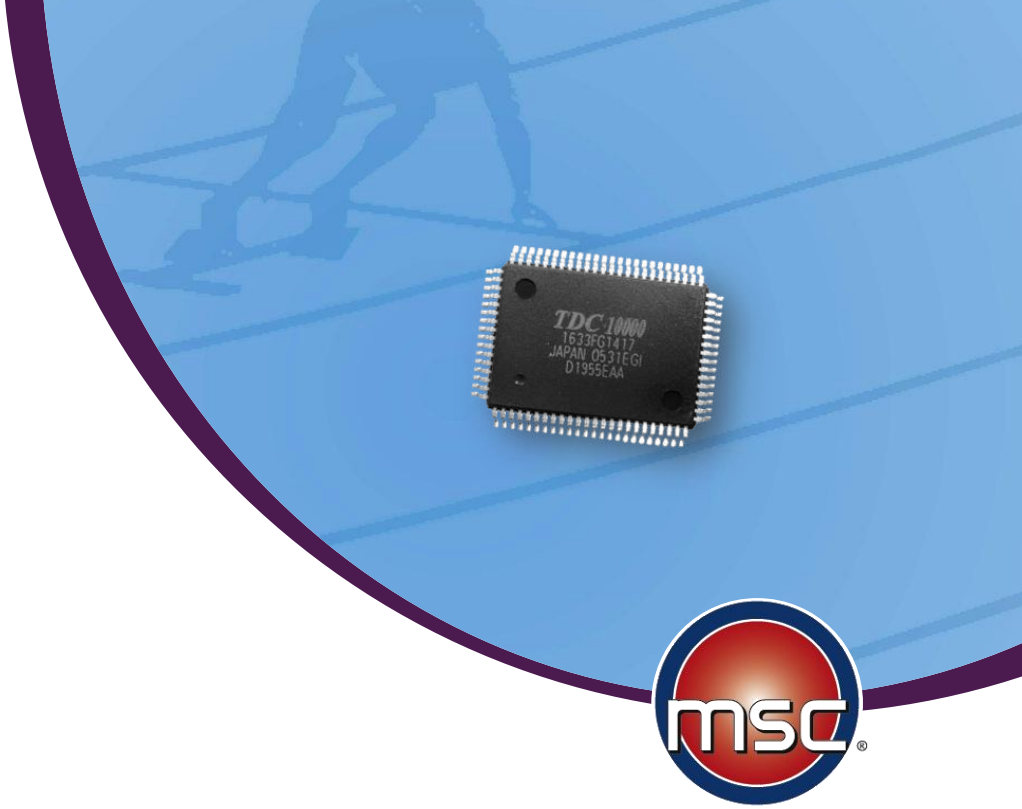

User Manual

MSC TDC10000

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1 Introduction

MSC Vertriebs GmbH has many years of experience in the development of high precision Time to Digital Converters (TDCs). MSC´s first TDC was developed in 1990 and implemented in a cost-effective Gate Array technology.

Similar to the terms ADC, DAC, etc., MSC established the term TDC (Time to digital Converter).

This manual describes the TDC10000, which is implemented in a 0,8µm-CMOS-process technology featuring 2.7V - 5V operation. The chip is delivered in a QFP80 0,8mm fine pitch package.

Supplied with 5V the TDC10000 achieves a typical resolution of 60ps. This resolution cannot be achieved using conventional time measurement components. The multi-channel function of the TDC10000 allows simultaneous measurement of time differences on two independent measurement channels.

The integrated measurement principle - together with the technology used - allows high-precision time difference measurement at low power consumption. The integration of the TDC10000 in battery-powered applications has become to a common procedure.

The TDC10000 is perfectly suited for measurement of time differences. Applications like distance measurement using laser, phase measurement, ultrasonic positioning, temperature measurement, etc. have been implemented successfully with our TDCs many times.

Please contact us! We are keen on satisfying your wishes.

2 Features

Channels:	two independent channels, each with one Start- and one Stop-input, programmable edge-sensitivity of the inputs, retriggerable Start-inputs
Resolution (5V, typ):	60ps
Measurement ranges: (5V, typ)	range I: short time measurement: 4ns - 6µs range II: long time measurement: 500ns - 8ms *)
Measurement modes:	4
Calibration clock:	external oscillator clock: 500 kHz - 10 MHz, internal programmable clock divider
Calibration measurement:	automatically after time measurement or stand-alone
Voltage range:	2.7V - 5.5V
Temperature range:	-40°C - 85°C
Processor interface:	8/16 bit selectable, status flags for interrupt generation, daisy chain for cascading of up to 31 TDCs
Internal memory:	FIFO for up to 4 measurement values per channel
Configuration:	software- and hardware configurable
Measurement improvement:	Auto Noise Unit
Resolution stabilisation:	Resolution-Lock Unit
Package:	PQFP80 with 0.8 mm pitch

**) Measurement range depends on period of calibration clock*

3 Block Diagram

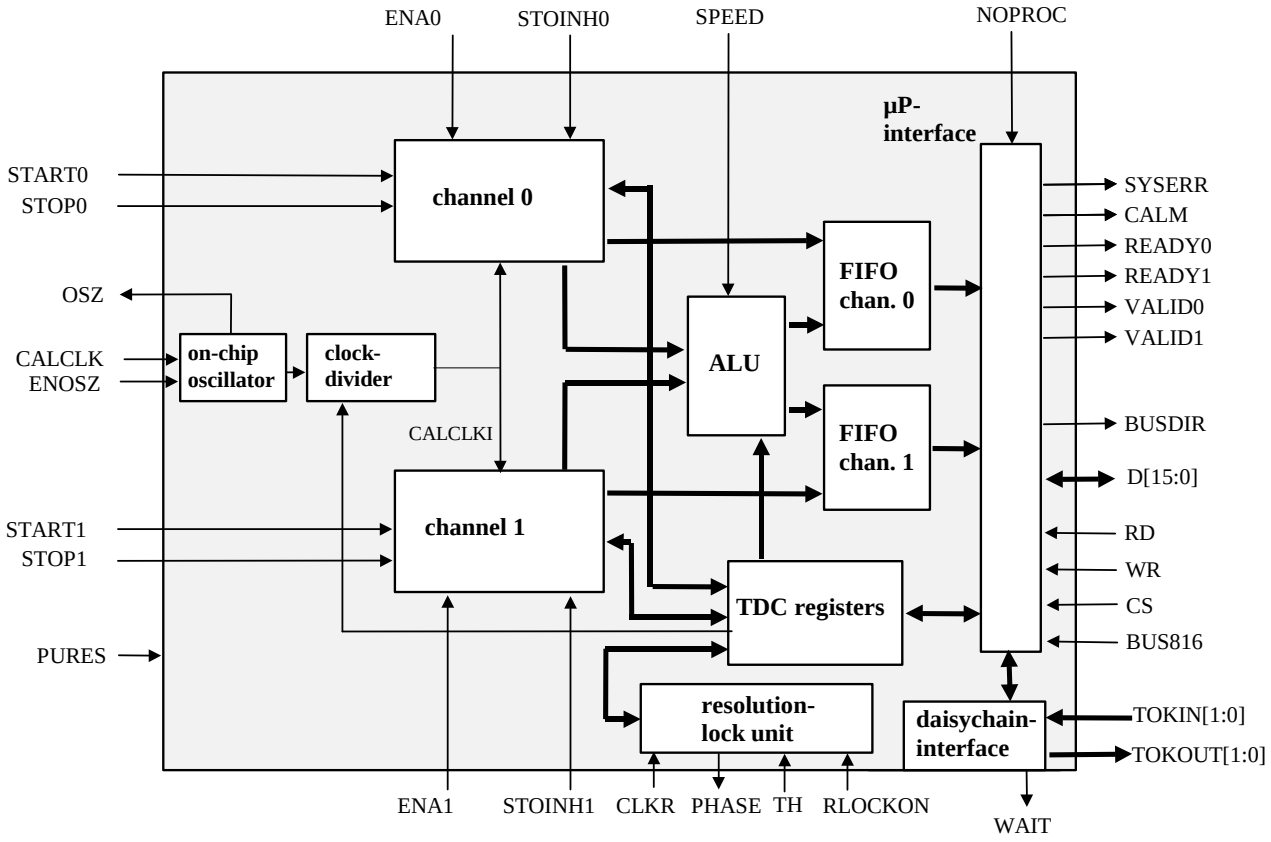

Figure 3.1: TDC10000 Block Diagram

The TDC offers two independent measurement **channels 0** and **1** for time measurement between the rising/falling edge of a signal at the start-input and the rising/falling edge of a signal at the stop-input with a typical resolution of 60ps (5V, 25°C). The measured values are processed within the **ALU** (Arithmetic Logical Unit). Up to four measurement values can be stored in the channel's Result-**FIFO** and read out via the **processor interface**.

The configuration of the TDC as well as the selection of the measurement mode and range is done by writing the **TDC-registers** via the processor interface. Status information can be accessed by reading the TDC registers.

The **resolution-lock unit** is used for stabilisation the TDC's resolution.

The **daisy chain interface** allows cascading of up to 31 TDCs.

The calibration clock, necessary for the calibration of the measurement values, has to be supplied by an external oscillator clock at the input CALCLK. The calibration clock is divided by the internal **clock divider**.

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4 Package and Pin Configuration

4.1 Package

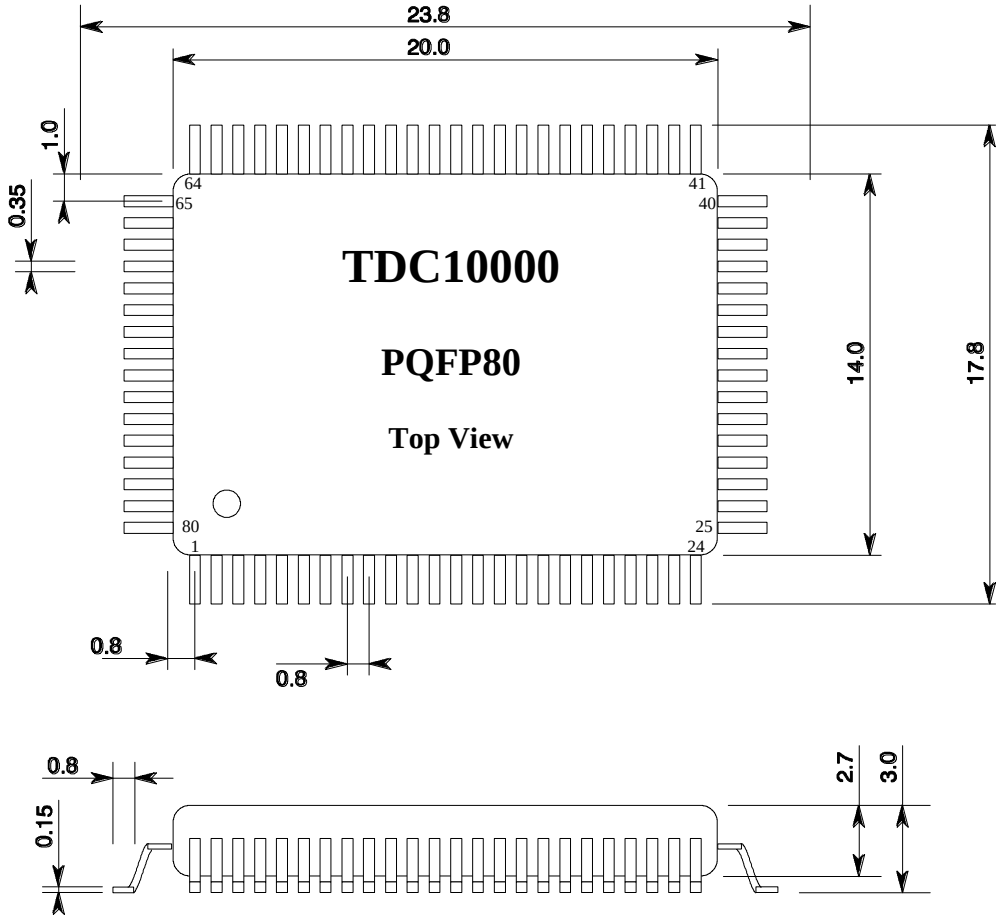

Figure 4.1: Package Dimensions (in mm)

4.2 Pin Configuration

Table 4.1 shows the TDC's pin configuration.

Pin No.	Pin name	I/O	Function
5, 11, 20, 25, 33, 51, 53, 73, 80	VDD	-	Supply voltage
4, 8, 12, 13, 21, 26, 29, 32, 39, 41, 50, 52, 54, 64, 72, 76, 79	VSS	-	Ground

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Pin No.	Pin name	I/O	Function
3, 22, 65	-	-	Unconnected
1	START0	In	Start-input channel 0
2	STOP0	In	Stop-input channel 0
6	ENOSZ	In	Enable calibration clock-input: 0: CALCLK-input enabled, can be disabled/enabled by software 1: CALCLK-input disabled, cannot be enabled by software
7	PHASE	Out, Slew Rate, 4mA	PLL phase discriminator output
9	OSZ	Out	Inverted output of the on-chip oscillators
10	CALCLK	In	Calibration clock-input: 500 kHz - 10 MHz
14	TH	In	Track/hold selection for PLL: 0: Track-Mode (default) 1: Hold-Mode
15	CLKR	In	Reference clock-input for PLL (default = 0)
16	RLOCKON	In	Resolution-lock unit: 0: off (default) 1: on
17	INHMD	In	Automatic M0-measurement: 0: off 1: on (default)
18	STOINH0	In	Stop inhibit channel 0: 0: STOP0-input enabled 1: STOP0-input disabled
19	STOINH1	In	Stop inhibit channel 1: 0: STOP1-input enabled 1: STOP1-input disabled
23	START1	In	Start-input channel 1
24	STOP1	In	Stop-input channel 1
27	ENA1	In	Enable channel 1: 0: channel 1 disabled, cannot be enabled by software 1: channel 1 enabled, can be disabled/enabled by software
28	BUS816	In	Processor interface: 0: 16-bit data bus 1: 8-bit data bus
30	WR	In	Write strobe (low active)
31	RD	In	Read strobe (low active)
34	SPEED	In	ALU-speed: 0: fast (default) 1: slow
35	CS	In	Chip select (low active)
36	TOKIN0	In	Token-input 0
37	TOKIN1	In	Token-input 1
38	NOPROC	In	Processorless mode: 0: off (default) 1: on
40	WAIT	Out, Open Drain, 8mA	WAIT-output for daisy chain read-sequence
42	D0	Bidi, 8mA	Bit0 data bus
43	D1	Bidi, 8mA	Bit1 data bus
44	D2	Bidi, 8mA	Bit2 data bus

Pin No.	Pin name	I/O	Function
45	D3	Bidi, 8mA	Bit3 data bus
46	D4	Bidi, 8mA	Bit4 data bus
47	D5	Bidi, 8mA	Bit5 data bus
48	D6	Bidi, 8mA	Bit6 data bus
49	D7	Bidi, 8mA	Bit7 data bus
55	D8	Bidi, 8mA	Bit8 data bus
56	D9	Bidi, 8mA	Bit9 data bus
57	D10	Bidi, 8mA	Bit10 data bus
58	D11	Bidi, 8mA	Bit11 data bus
59	D12	Bidi, 8mA	Bit12 data bus
60	D13	Bidi, 8mA	Bit13 data bus
61	D14	Bidi, 8mA	Bit14 data bus
62	D15	Bidi, 8mA	Bit15 data bus
63	BUSDIR	Out, Open-Drain, 8mA	Bus direction indicator: 0: when RDN = 0 (data direction is Out), HiZ: else (data direction is In), pull-up resistor necessary
66	TOKOUT1	Out, High-Speed, 4mA	Token-output 1
67	TOKOUT0	Out, High-Speed, 4mA	Token-output 0
68	CALM	Out, 4mA	0: at least one measurement is running at the moment 1: no measurement is running at the moment
69	READY0	Out, 4mA	0: channel 0 not ready for measurement 1: channel 0 ready for measurement
70	READY1	Out, 4mA	0: channel 1 not ready for measurement 1: channel 1 ready for measurement
71	SYSERR	Out, 4mA	0: TDC ok 1: overflow error (channel independent)
74	VALID0	Out, 4mA	0: channel 0 has no valid measurement results for readout 1: channel 0 has valid measurement results for readout
75	VALID1	Out, 4mA	0: channel 1 has no valid measurement results for readout 1: channel 1 has valid measurement results for readout
77	PURES	In	Power-on reset (high active)
78	ENA0	In	Enable channel 0: 0: channel 0 disabled, cannot be enabled by software 1: channel 0 enabled, can be disabled/enabled by software

Remarks:

- *Connect all unused inputs to GND.*
- *Data bus DATA[15:0] is not allowed to float: please pull up or down (with e.g. 10kΩ).*
- *Do not connect unused outputs.*
- *All inputs are TTL.*

Table 4.1: Pin Description

5 Measuring Procedure

The TDC10000 provides two identical measurement channels, each with a typical resolution of 60ps at 5V and 25°C. The figures of the user manual always refer to channel 0, however they apply equally well to channel 1.

5.1 Time Difference Measurement

As shown in Figure 5.1, per channel one edge sensitive start- and one edge sensitive stop-input are used for measuring the time difference t_{VAL}. The *time measurement* in the measuring core of the respective channel is started by a start-signal and ended by a stop-signal. The internal ALU calculates the measurement value VAL which is stored in the Result-FIFO of the appropriate channel.

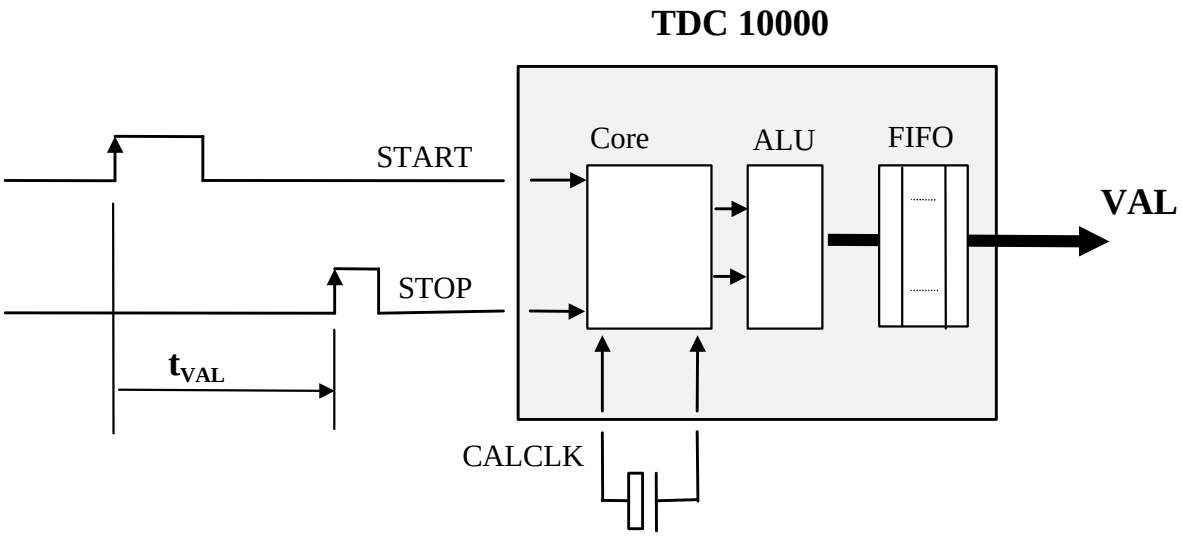

Figure 5.1: Time Difference Measurement

The measurement value VAL is dependent on the temperature and the supply voltage. It therefore has to be weighted according to the TDC characteristic (measurement straight, Figure 5.2). Offset and grade of the characteristic have to be determined by a so-called *calibration measurement*. This can be executed immediately after every time measurement.

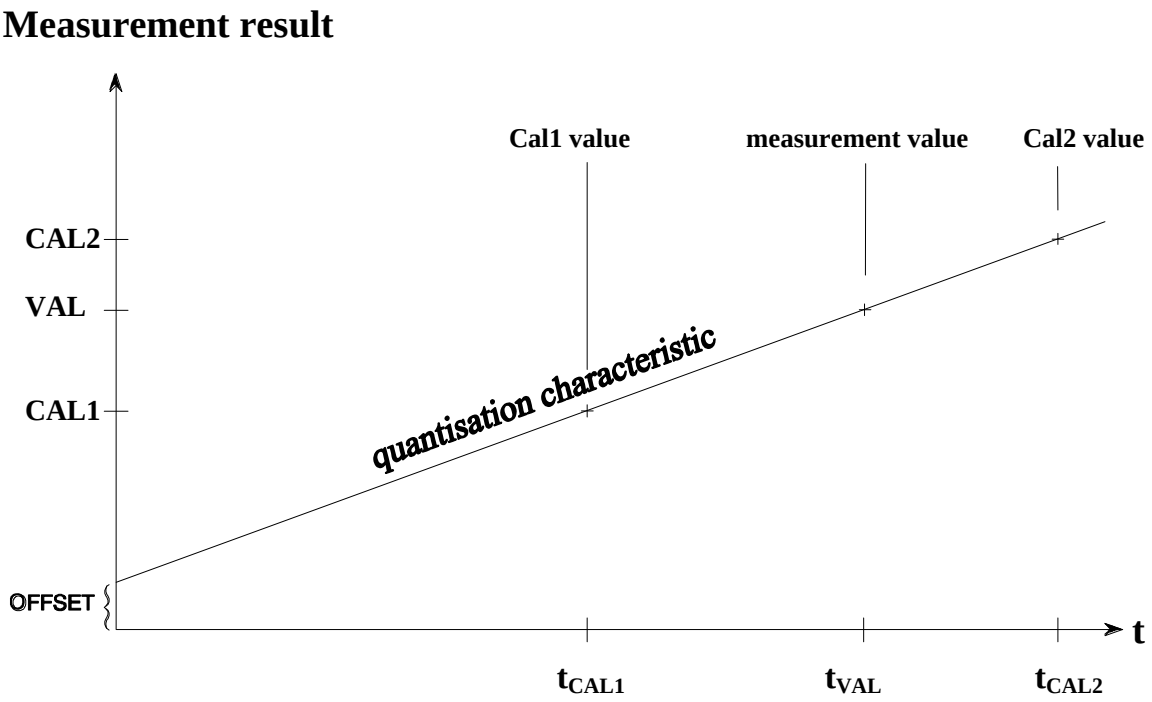

Figure 5.2: Characteristic of the TDC Core

5.2 Generating Calibration Values

Only one calibration clock CALCLK has to be provided for calibration measurements of both channels. This clock is the absolute time reference and therefore must have the precision of a quartz crystal. The calibration clock is divided by an internal calibration clock divider. The resulting clock CALCLKI is used as internal reference clock and measured by both measuring cores.

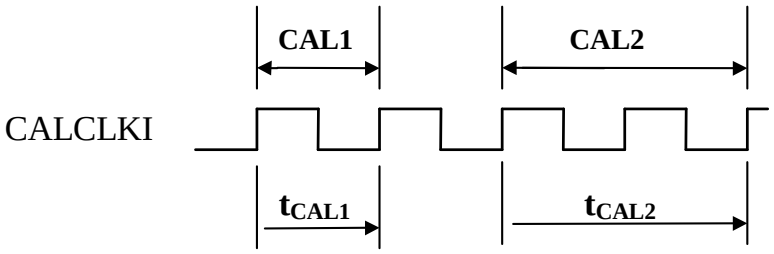

Figure 5.3: Calibration Measurement

During the calibration measurement the length of one and two periods of the divided calibration clock (t_{CAL1}, t_{CAL2}) are measured and the resulting calibration values CAL1 and CAL2 are stored just like the measurement value VAL in the Result-FIFO of the respective measurement channel. The time values t_{CAL1} and $t_{CAL2} = 2 * t_{CAL1}$ are well known.

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5.3 M0-Measurement

Measurement- and calibration- values of each channel are standardized in the ALU using the TDC-specific internal characteristic quantity, called M0. M0 is generated using the measuring core of the appropriate channel.

In order to minimize the influences of temperature and supply voltage and to optimize the precision of measurement, a M0-measurement has to be executed just like a calibration measurement in cyclic temporal distances.

5.4 Measurement Ranges

The TDC provides two measurement ranges, individually programmable for each channel:

- Range I: uses the TDC-core for short time measurement: 4ns - 6µs *)
- Range II: uses the TDC-core and the precounter for long time measurement: 500ns - 8ms *) **)

*) *typical at 5V, 25°C*

**) *Measurement range depends on period of calibration clock*

5.4.1 Measurement Procedure in Measurement Range I

In the measurement range I the measurement value VAL between the start-and the stop-signal of a time measurement is determined using the measuring core of the respective channel.

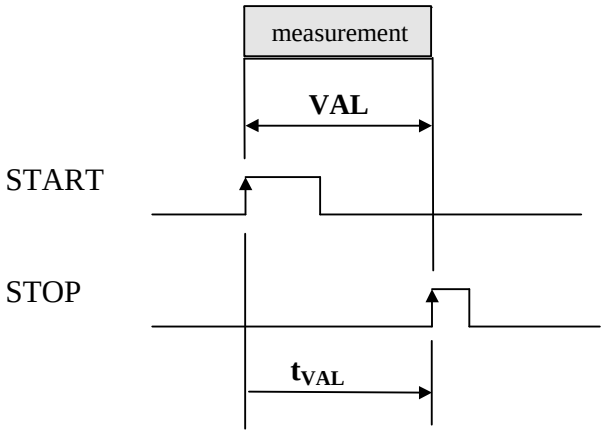

Figure 5.4: Measurement in Measurement Range I

The measured time t_{VAL} is calculated using the clock period time t_{CAL1} of the divided calibration clock and the TDC's measurement results VAL, CAL1 and CAL2 in accordance with the TDC characteristic (see Figure 5. 2) as follows:

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$$(1) \quad t_{VAL} = \frac{VAL - Offset}{CAL2 - CAL1} * t_{CAL1}$$

$$(2) \quad Offset = 2 * CAL1 - CAL2$$

5.4.2 Measurement Procedure in Measurement Range II

In the measurement range II a time measurement is divided into three partial measurements in accordance with Figure 5.5:

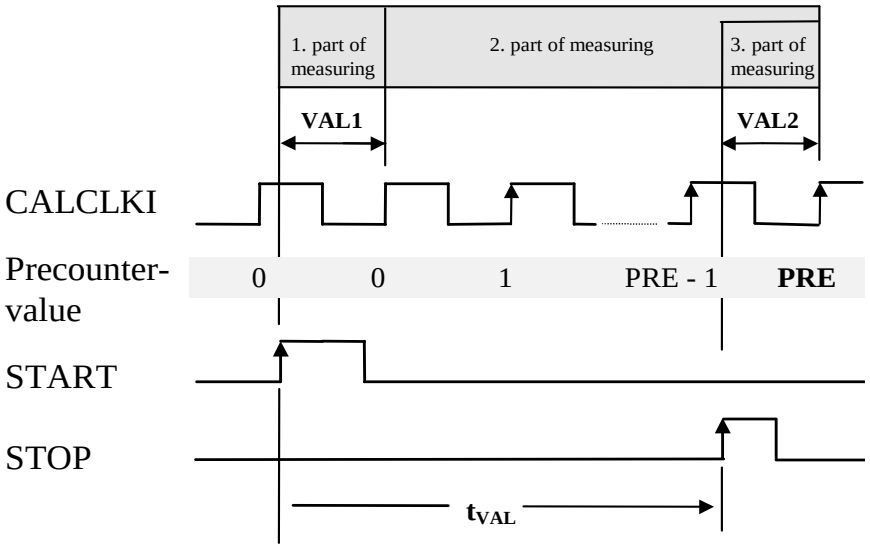

Figure 5.5: Measurement in Measurement Range II

In the first part of measurement, the value **VAL1** representing the time between the start-signal and the next rising edge of the divided calibration clock is measured using the measuring core of the respective channel. In the second part of measurement, the integral number **PRE** of calibration clock periods between the start- and the stop-signal is determined by the so-called *precounter* of the channel. In the third part of measurement, the measurement value **VAL2**, which represents the time between the stop-signal and the next rising edge of the calibration clock, is measured using the measuring core once more.

The measured time t_{VAL} is calculated using the clock period time t_{CAL1} of the divided calibration clock and the TDC's measurement results VAL1, VAL2, PRE, CAL1 and CAL2 in accordance with the TDC characteristic (see Figure 5. 2) as follows:

$$(3) \quad t_{VAL} = \left(\frac{VAL1 - VAL2}{CAL2 - CAL1} + PRE \right) * t_{CAL1}$$

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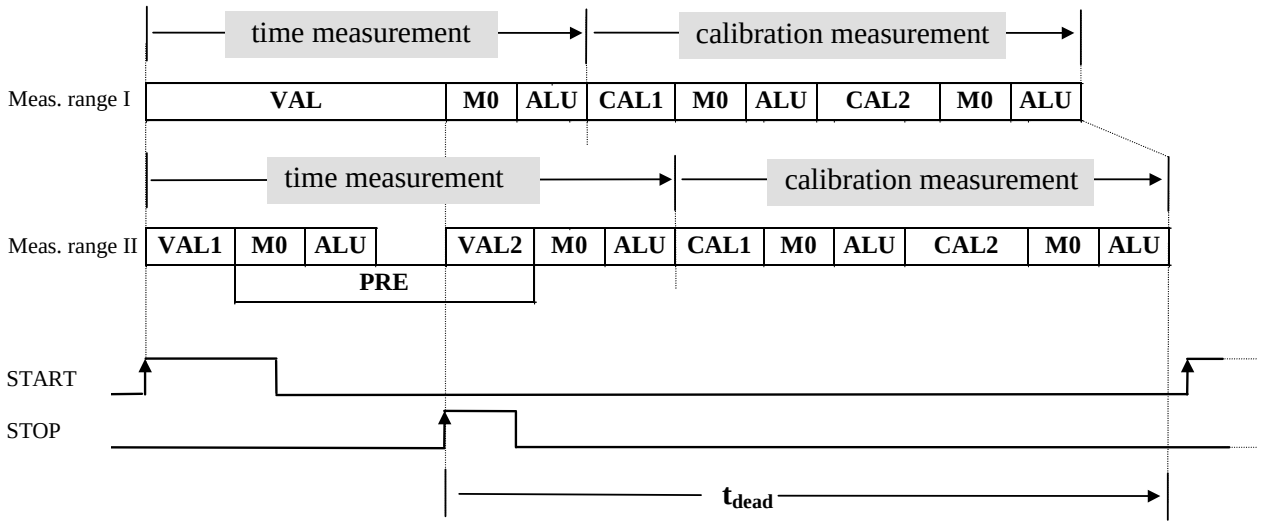
5.5 Measurement Modes

Figure 5.1 shows the general measurement cycle including the ALU-processing for both measurement ranges:

A time measurement is completed by the occurrence of a start-signal followed by a stop-signal. Depending on the measurement mode a calibration measurement follows automatically. It's also possible to execute a calibration measurement 'separately' without a prior time measurement.



VAL:	Generation of measurement value VAL in measurement range I
VAL1, VAL2:	Generation of measurement values VAL1 and VAL2 in measurement range II
PRE:	Generation of precounter value PRE in measurement range II
M0:	Generation of TDC-characteristic quantity M0
CAL1:	Generation of calibration value CAL1
CAL2:	Generation of calibration value CAL2
ALU:	ALU-processing
t_{dead}:	dead time of measurement

Figure 5.1: General Measurement Cycle

Normally, after generating a measurement- or calibration value, a new M0 is generated, too. This automatic M0-measurement can be disabled by software. If doing so, 'separate' M0-measurements have to be performed via software - similar to separate calibration measurements.

As shown in Figure 5.1 the TDC has got a so-called *dead time* t_{dead} after the arrival of the time measurement's stop-signal. During this dead time all start-and stop-signals are ignored due to the measurement principle of the TDC10000. Depending on the configuration and the measurement mode selected this time differs within a wide range. After dead time the channel is ready again for measurement at the earliest and accepts start-and stop-signals for a new measurement. The maximun dead times expected are shown in Chapter 8.4, Dead Times.

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In Table 6.1 all measurement modes of the TDC10000 are shown. They are selectable for each channel independently by software.

Measurement mode	Measurement range	Calibration measurement	Sequence of the measurement results stored in the Result-FIFO
0: Default Mode	I	automatic	VAL, CAL1, CAL2
1: High-Speed Mode	I	no	VAL
2: Separate calibration measurement	I	-	CAL1, CAL2
3: Long time measurement	II	automatic	VAL1, VAL2, CAL1, CAL2, PRE

Table 5.1: Measurement Modes

Notes:

1) *After power-on reset the TDC is in measurement mode 0.*

2) *In the measurement mode 1 separate calibration measurements have to be executed via measurement mode 2.*

3) *In measurement mode 2 the channel switches to the default mode (measurement mode 0) after completion the generation of the calibration values. Since measurement mode 2 co-operates with measurement mode 1, you have to renew mode 1 via software.*

4) *The precounter value PRE is stored in a separate register.*

5) *The readout of the results in measurement mode 3 has to be performed 'En Bloc'. This means that no readout should take place until the stop-value VAL2 is stored in the Result-FIFO, even though the VALID signal is set to '1' indicating that the start-value VAL1 is present in the Result-FIFO. Reason: When reading out VAL1 too early the Result-FIFO runs empty and causes the read instruction to be cancelled. When the read instruction is renewed for reading out the remaining measurement results the precounter value is lost and can't be read out!*

6 Functional Description

6.1 On-Chip Oscillator

For the generation of the calibration clock the TDC provides a so-called on-chip oscillator. As represented in Figure 6.1, the TDC oscillator circuit consists of an inverting amplifier element only. The external components consist of one quartz crystal, two capacitors C1 and C2, and one resistor Rf.

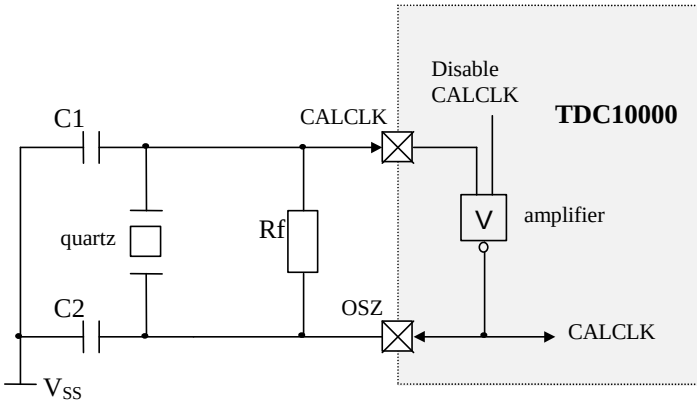

Figure 6.1: On-Chip Oscillator

If the on-chip oscillator is not used, then an externally generated clock has to be connected to pin CALCLK. In this case the pin OSZ is not connected. The calibration clock-input CALCLK is enabled or disabled by the pin ENOSZ. If the calibration clock-input is enabled by ENOSZ it can also be enabled and disabled by software.

6.2 Calibration Clock Divider

Figure 6.2 shows the principle function of the calibration clock divider.

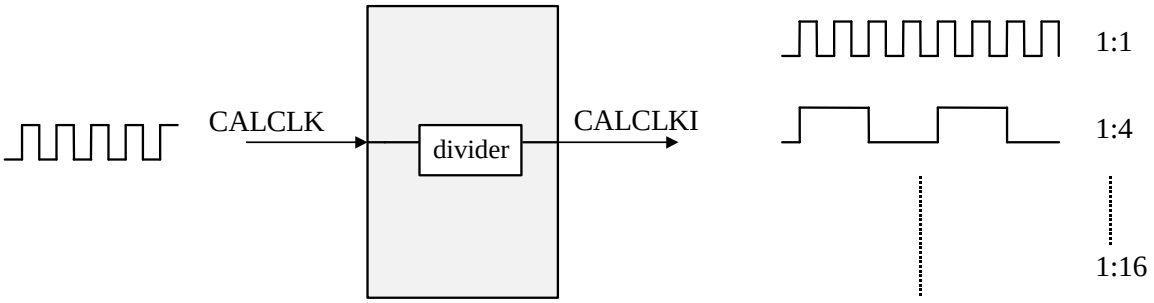

Figure 6.2: Calibration Clock Divider

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The external calibration clock CALCLK is divided by the TDC's calibration clock divider. The division factors are programmable and can be 1, 4, 8 and 16.

Since calibration measurements are always done by a TDC's measuring core, it is necessary to ensure that the clock period of the divided calibration clock is not larger than 3µs (5V, typ), otherwise the measurement of two calibration clock periods would cause a measurement range overflow.

In order to achieve high precision accuracy, when measuring in the measurement range I, the division factor should be selected in such a way, that the time difference t_{VAL} to be measured is in the range of two calibration clock periods.

To achieve best measurement results in the measurement range II the period of the divided calibration clock should be as long as possible.

6.3 Measurement Channels

Figure 6.3 shows the block diagram of the measurement channels.

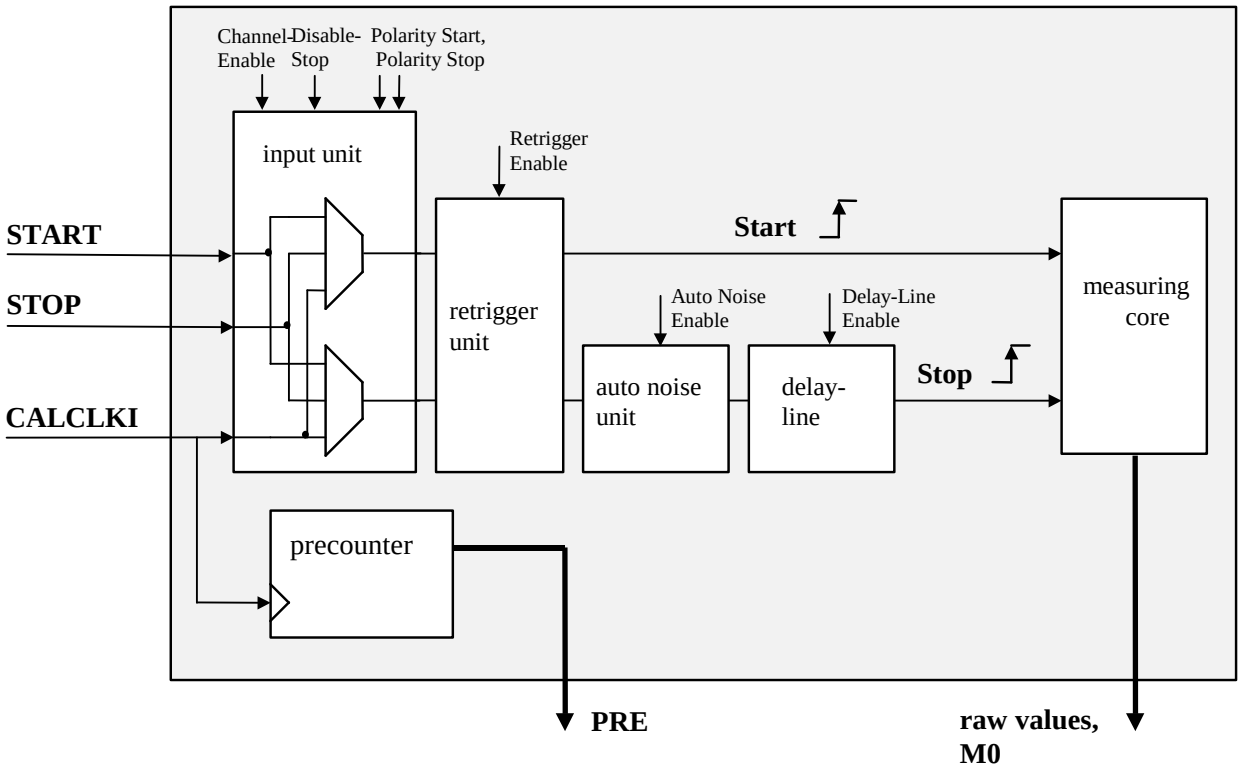

Figure 6.3: Measurement Channel Block Diagram

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6.3.1 Input Unit

The input unit handles the incoming start-, stop- and calibration clock-signals using the following control signals:

- Channel-Enable:

  The measurement channels are enabled/disabled using the pins ENA0 and ENA1. If a channel is disabled, no start-, stop-, or calibration clock-signals will reach the measuring core and no measurement will take place. If the measurement channels are enabled by ENA0 and ENA1, they can also be enabled/disabled by software.

- Inhibit-Stop:

  With the pins STOINH0 and STOINH1 the stop-inputs STOP0 and STOP1 of the channels can be disabled. No stop-signals will be passed to the measuring core.

- Polarity Start / Polarity Stop:

  The edge-sensitivities of the start- and stop-inputs are adjusted independently from each other and separately for the two channels by software. The input unit of each channel therefore triggers on rising or falling edges of the start- and stop-signals depending on the configuration.

Furthermore the input unit decides, which signal (start, stop or calibration clock) has to be passed on as a start- or stop-signal to the measuring core, depending on the measurement mode and on the partial step of the measurement cycle.

6.3.2 Retrigger Unit

If the retrigger unit is enabled, the measurement is re-started at the appearance of every start at the channel's start-input as long as no stop has been detected at the channel's stop-input. As shown in Figure 6.4, the determined time difference is the time between the *last* start-signal and the stop-signal. If the Retrigger Unit isn't enabled then the time between the *first* start and the stop-signal is measured.

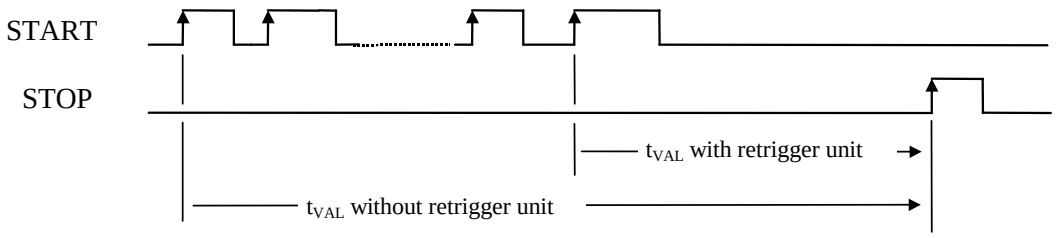

Figure 6.4: Measurement with and without Retrigger Unit

Please note, that a retriggering start-signal should occur 30ns (5V, typ) after a previous start-signal at the earliest. The retrigger unit can be enabled by software independently for both channels in the measurement modes 0 and 1 (measurement range I).

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6.3.3 Auto Noise Unit

The characteristic of the TDC is a straight line with offset and upward gradient, which due to the digital measurement procedure possesses quantisation stages – so called LSBs (Least Significant Bits) - with the width of the resolution. For a single measurement one therefore gets a quantisation error of up to one quantisation stage at ideal quantisation. This precision is sufficient for most applications.

A higher precision can be achieved when the measurement of the same time is repeated several times and statistical methods are used:

Changing the existing offset of the characteristic for each single measurement by delaying the stop-signal according to Figure 6.5 causes sampling at different positions of the characteristic, especially when measuring very constant time differences of a low noise signal. If the same offset shift is still present during generation of the calibration values for the associated measurement value, the total offset is eliminated during the time difference calculation according to the formulas (1) and (2). When averaging all the single measurements, there quantisation errors are averaged as well.

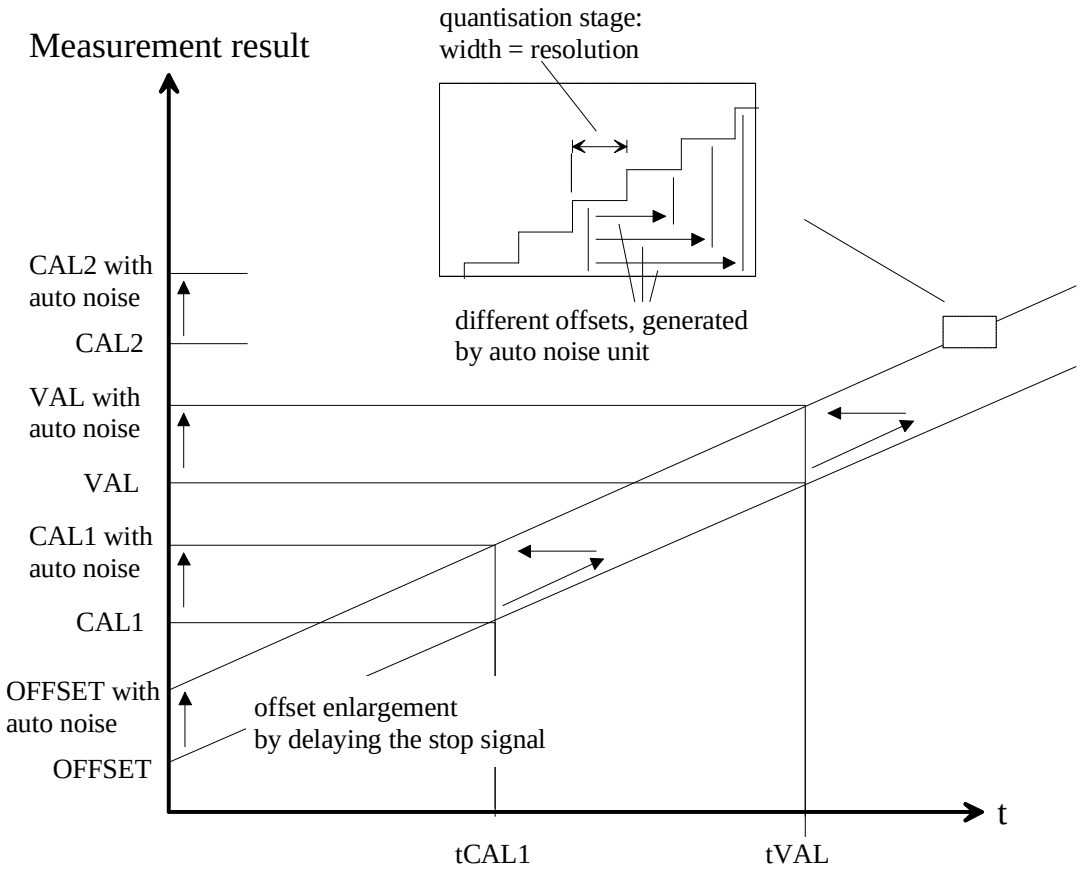

Figure 6.5: Influence of the Auto Noise Unit on the Characteristic of the TDC Measuring Core

If the auto noise unit is enabled a channel specific delay is generated by a pseudo-random number generator. This delay is changed with every new measurement and added to the already existing offset of the respective channel. The auto noise unit is available only in the measurement modes 0 and 3.

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6.3.4 Delay-Line

When the delay-line is enabled by software, an additional offset of approx. 100ns (5V, typ) is generated for both channels. Due to transient effects, delaying the channel's stop-signal often leads to a higher precision accuracy when measuring time differences <20ns.

An enabled delay-line will also increase the channel's dead time by the amount of offset.

6.3.5 Measuring Core

The measuring core of a channel determines the time interval between a start- and a stop-signal with a typical resolution of 60ps (5V, 25°C). The measuring core then provides measurement or calibration values as raw values to the ALU for further processing.

In addition, depending on the TDC's configuration the core generates the TDC-specific characteristic quantity M0 for each raw value. M0 is stored in the M0-Register of the respective channel for further processing by the ALU.

It can be selected by software, whether the measuring core generates M0 with 1-fold or with 16-fold accuracy. The generation of M0 with 16-fold accuracy takes 16 times longer than the generation of M0 with 1-fold accuracy. Higher accuracy of M0 thus causes a greater dead time of the measurement.

6.3.6 Precounter

Within the measurement range II the precounter of each measurement channel counts the clock periods t_{CAL} of the divided calibration clock CALCLKI between the start-signal and the stop-signal of the time measurement. The precounter value PRE is 12 bit. This results in a maximum measurement period of $t_{cal} * 2^{12}$ in the measurement range II.

6.4 Arithmetical Logic Unit (ALU)

The ALU is a flash based ALU. It calculates the measurement and calibration values of both channels using the raw values of a measurement and the associated characteristic quantity M0. The results are stored in the Result-FIFO of the respective channel.

In order to exclude an influence on measurements by ALU-calculations taking place at the same time, in the measurement range I a suppression of ALU-calculations can be enabled during running measurements by software.

If suppression is enabled, any measurements on both channels are suppressed during running ALU-calculations as well, since both measurement channels are disabled during this time.

6.5 Resolution-Lock Unit

The TDC10000 provides a resolution-lock unit. This unit allows the TDC's resolution to be kept almost constant (approx. 0,003%/K) by using a closed-loop control of the supply voltage. If the resolution-lock unit is activated, the calibration values once generated, can be used further on. Calibration measurements are no longer required if large variations in temperature do not occur.

6.5.1 Principle Function

In order to keep the temperature- and voltage-dependent resolution of the TDC constant, one needs a 'run time sensor' on the chip which recognizes and compensates for any fluctuations. For this purpose a ring oscillator is used. Its frequency is temperature- and voltage-dependent in the same manner as the resolution of the measuring cores. The ring oscillator is used as the VCO of a PLL and the generated clock is compared with a (quartz exact) clock supplied externally via pin CLKR. So the clock of the ring oscillator and the resolution of the TDC are kept constant by a controlled variable for the supply voltage derived from the PLL.

6.5.2 Operating Sequence

Figure 6.6 shows the TDC-internal part of the PLL. The resolution-lock unit has two functional modes, *Track* and *Hold*. These modes are selected by pin TH or by software.

Activating the resolution-lock unit is done either by software within the register GLOBREG0 or by setting pin RLOCKON to '1'.

Track-Mode:

This mode is used for the adjustment of the PLL in the Hold-Mode: The period of the reference clock CLKR, divided by four, is counted out by the ring oscillator clock. The determined multiplication factor of the ring oscillator clock to the reference clock is stored in the Latch 8 with about 8 bits of precision. Latch 8 is updated each period of the reference clock/4. When the temperature is rising on the chip the multiplication factor will decrease, when the temperature is falling the factor will rise.

During Track-Mode the resolution-lock function is not activated. A rectangle waveform with a pulse/mark-ratio of 1:1 is generated at the phase discriminator output (pin PHASE). Its frequency is 1/8 of the reference clock. For thermal stabilisation of the chip it makes sense to activate this mode approx. 5 minutes before changing to the Hold-Mode.

Hold-Mode:

In this mode the PLL is active. The value stored in the Latch 8 is used as multiplication factor for the ring oscillator clock. The clock is multiplied by this factor and compared with the reference clock/4 within the phase discriminator. The result forms the phase discriminator output signal. It's a rectangle with variable pulse/mark-ratio. This signal can be used (low-pass-filtered) as analog controlled variable of the analog part of the PLL, which has to be realised externally. With the TDC-external analog part controlling the supply voltage of the TDC10000 and the frequency of the ring

oscillator, the loop control of the PLL is closed: When the temperature is falling on the chip the supply voltage will decrease, when the temperature is rising the supply voltage will rise, too.

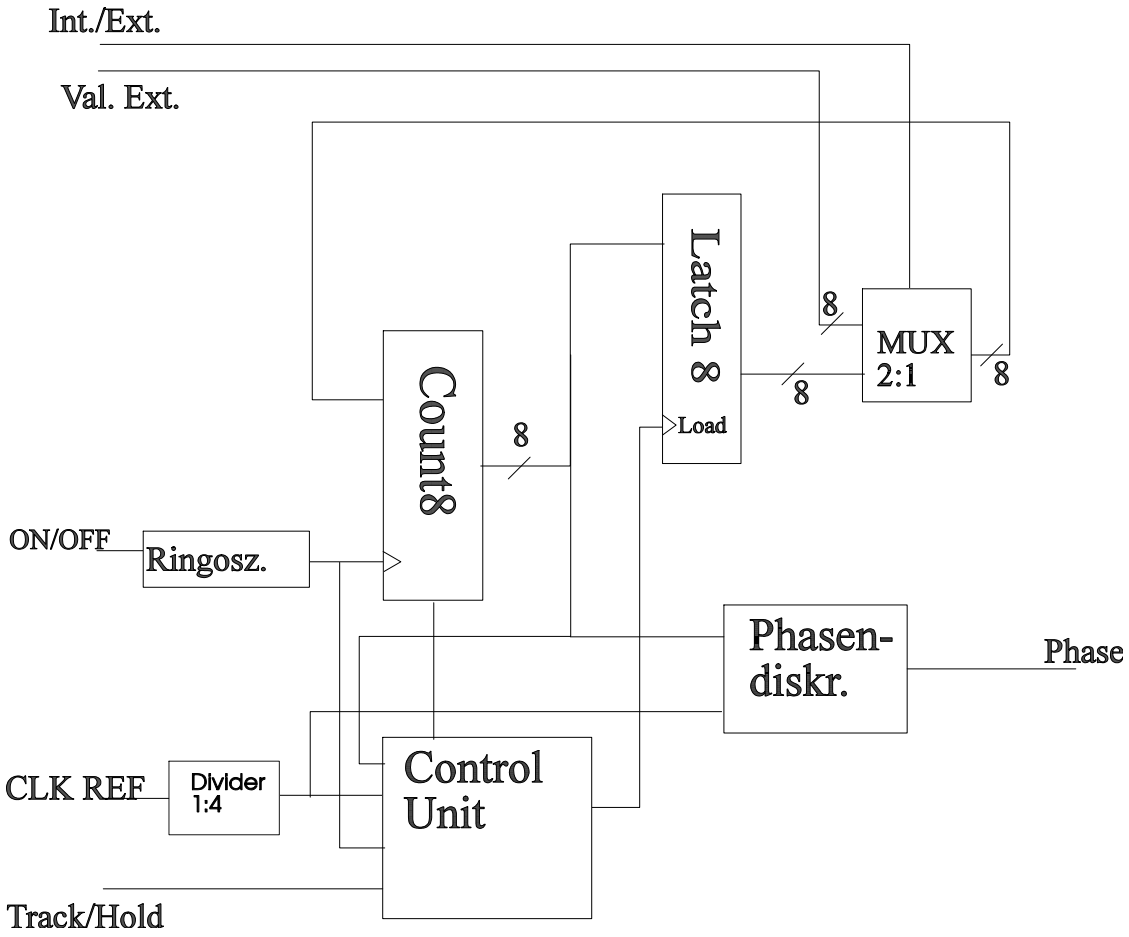

Figure 6.6: TDC-internal Part of the PLL

The value of the Latch 8 can be read out via the processor interface. Furthermore there is the possibility of using an external multiplication factor instead of the internal value of Latch 8. This external factor has to be written into the register LOCKREG.

Using an external multiplication factor some interesting applications are possible:

- Once adjusted, the resolution is accurately reproducible (quartz accuracy) at any time by rewriting the same multiplication factor. In this way different environmental conditions can be compensated for a whole series of measurements.
- For multi-TDC applications it is possible to tune the resolution of several TDC10000 with a precision of up to ±0,5% to each other.

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6.5.3 Resolution-Lock Unit Registers

The resolution-lock unit has two registers for configuration:

6.5.3.1 LOCKMOD Register

In this register the usage of the internal or external multiplication factor is selected and the resolution-lock unit is adapted to the reference clock and to the external loop filter. The width of this register is 8 bit. For detailed information on the individual register bits refer to Chapter 7.3.5, LOCKMOD Register.

6.5.3.2 LOCKREG Register

When using an external multiplication factor instead of the internal value of Latch 8, this factor has to be written into the LOCKREG Register. The width of the register is 8 bit (see also Chapter 7.3.6, LOCKREG Register).

6.5.4 External Analog Circuit

The PLL consists of internal and external components. The loop filter and the closed-loop voltage control of the TDC10000 have to be realised with external components. Figure 6.7 shows a possible external analog circuit, designed for 12V supply voltage.

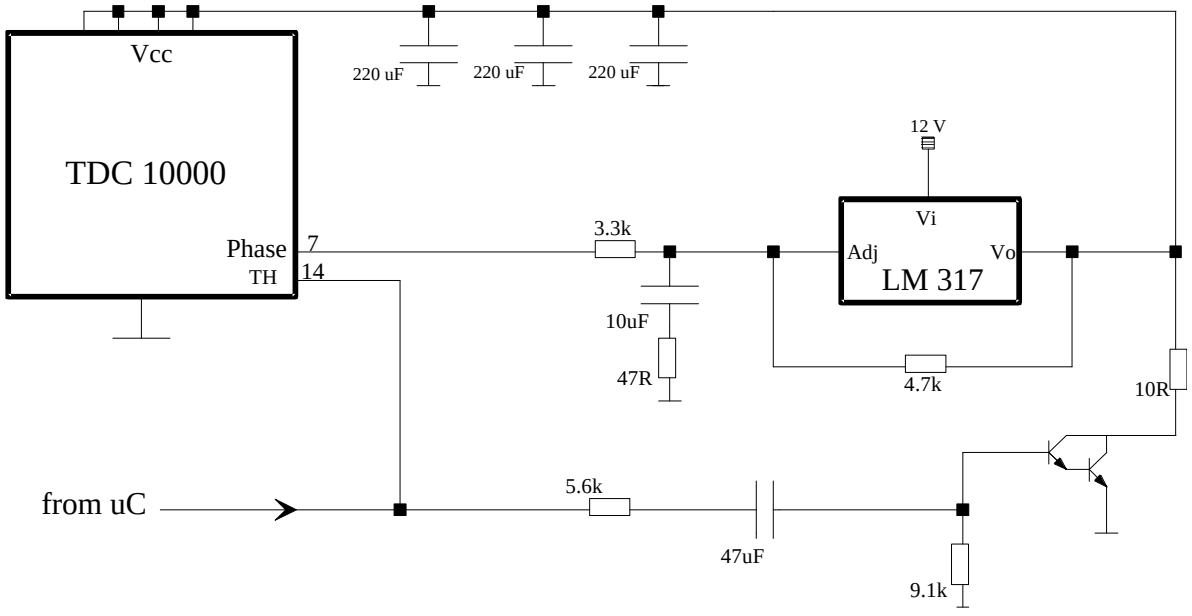

Figure 6.7: TDC-external Part of the PLL

6.5.5 Power Consumption

Normally, when the resolution-lock unit isn't enabled the quiescent current of the TDC10000 is in the range of nanoamperes. When the resolution-lock unit is activated the ring oscillator will cause a quiescent current consumption of approx. 20mA. In addition, the external circuit will increase the quiescent current consumption.

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6.6 TDC Registers

6.6.1 Instruction Register

The configuration of the TDC, the readout of measurement results or the TDC's status is controlled by instructions that are written into the Instruction Register. A detailed description of the TDC instructions can be found in Chapter 7.1, Execution of Instructions.

6.6.2 Mode Registers

The TDC provides two Mode Registers, one for the configuration of channel 0 and one for the configuration of channel 1. The width of the registers is 8 bit. In these registers the measurement mode as well as the edges of the start- and stop-signals, on which the respective channel will trigger, are selected. So it's possible to set up one channel to measure a large time difference and at the same time the other channel to measures the pulse width of the much shorter start- or stop-pulse. A detailed description of the individual register bits is given in Chapter 7.3.1, Mode Registers MODREG0/1.

6.6.3 Global Registers

There are two Global Registers for configurations concerning both channels. The width of these registers is 8 bit. Here the division factor for the calibration clock divider is selected, the automatic M0-measurement can be disabled and the resolution-lock unit is activated. Furthermore the daisy chain is configured here. For detailed information on the individual register bits refer to Chapter 7.3.2, Global Register GLOBREG0 and Chapter 7.3.3, Global Register GLOBREG1.

6.6.4 Offset Registers

There is one Offset Register for each channel. The width of these registers is 8 bit. Here a correction value is stored for the ALU, to prevent the ALU going into overflow when measuring very small time differences on the respective channel. (see also Chapter 7.3.4, Offset Registers OFFSET0/1).

6.6.5 Status Register

The Status Register of the TDC reflects the present status of the TDC. It contains six status flags, which are described in detail in Chapter 6.8.2, Status Flags.

6.6.6 M0-Registers

Both measurement channels have their own M0-Register in which the characteristic quantity M0 generated by the respective measuring core is stored for further processing by the ALU. If M0 is not generated automatically during a measurement then M0 can also be generated and stored executing a separate M0-measurement.

6.7 Result-FIFOs

Both measurement channels have a Result-FIFO for up to 4 measurement results (= measurement and/or calibration values) calculated by the ALU and stored for readout via the processor interface.

When a FIFO is full the corresponding channel is disabled until at least one measurement result is read out. When a FIFO is empty the read instruction for the corresponding channel is ignored.

6.8 Processor Interface

For the communication with a microprocessor the TDC provides a processor interface shown in Figure 6.8.

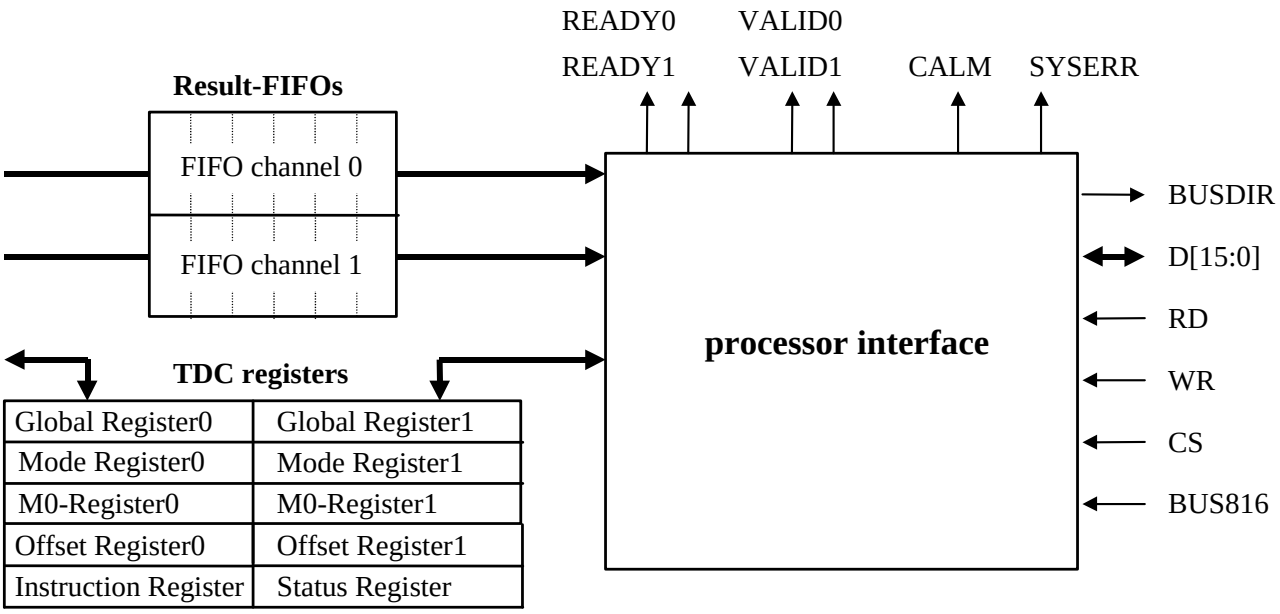

Figure 6.8: Block Diagram Processor Interface

Via the processor interface the access to all TDC registers (Instruction Register, Mode Registers, Global Registers, Status Register, Offset Registers and M0-Registers) is performed as well as the access to the registers of the resolution-lock unit and the Result-FIFOs of both channels.

In addition to data- and control lines the processor interface provides six status flags for interrupt generation at the connected processor.

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6.8.1 Data- and Control Lines

6.8.1.1 Overview

The TDC 10000 provides the following data- and control-lines:

- D[15:0]: Bi-directional data bus
- CS: Chip select (low active)
- RD: Read strobe (low active)
- WR: Write strobe (low active)
- BUSDIR: Indicates the current bus direction

For optimal adjustment to the data structure of the connected processor and its data bus width, the width of the TDC's data bus is set to 8 bits (8-bit mode) or 16 bits (16-bit mode) by the pin BUS816.

6.8.1.2 Timing Diagrams

Figure 6.9 shows the timing for read and write cycles. Please notice that in 8-bit mode the data lines D[15..8] remain High-Z at all times.

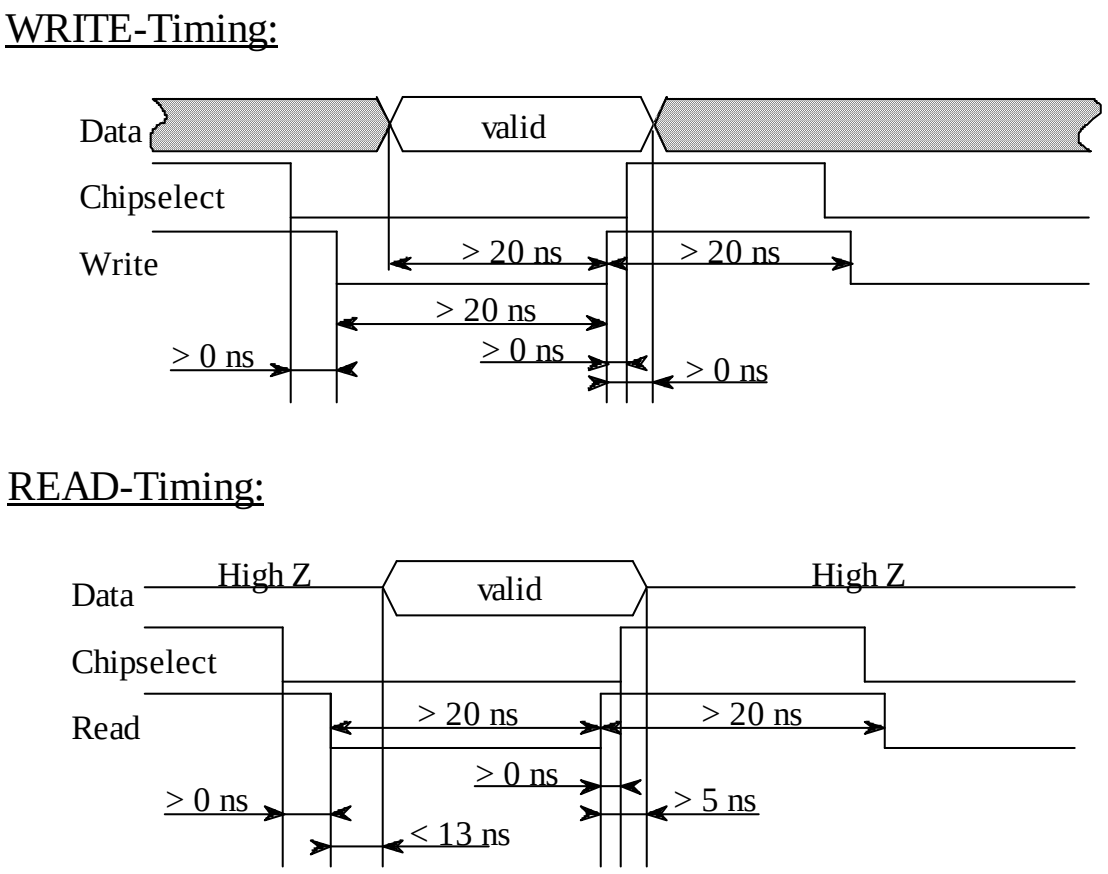

Figure 6.9: READ- and WRITE-Timing of the Processor Interface (typical at 5V, 25°C)

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6.8.2 Status Flags

For interrupt generation at the connected processor the TDC provides six status pins:

- READY0: Channel 0 ready for measurement
- READY1: Channel 1 ready for measurement
- VALID0: Channel 0 has valid measurement results for readout
- VALID1: Channel 1 has valid measurement results for readout
- SYSERR: Overflow error (channel independent)
- CALM: TDC is calm: no measurement is running at the moment

All status pins are described in Table 6.1. They are identical with the status flags of the Status Register and therefore can be read by software, too.

Channel 0			Channel 1		
READY0	0:	Channel not ready, measurements cannot be started, because start-input START0 is disabled.	**READY1**	0:	Channel not ready, measurements cannot be started, because start-input START1 is disabled.
	1:	Channel is ready for measurement (default) and waits for a start-signal. If the retrigger unit is enabled, the channel remains ready until a stop-signal occurs.		1:	Channel is ready for measurement (default) and waits for a start-signal. If the retrigger unit is enabled, the channel remains ready until a stop-signal occurs.
VALID0	0:	Result-FIFO of channel 0 is empty. No measurement results for readout (default).	**VALID1**	0:	Result-FIFO of channel 1 is empty. No measurement results for readout (default).
	1:	Result-FIFO of channel 0 has at least one valid measurement result (VAL, VAL1, VAL2, CAL1, CAL2, PRE*) for readout.		1:	Result-FIFO of channel 1 has at least one valid measurement result (VAL, VAL1, VAL2, CAL1, CAL2, PRE*) for readout.
SYSERR	0:	No overflow error (default).			
	1:	Overflow of one or both channels. If the retrigger unit is enabled, the next retriggering start-signal clears SYSERR to ‘0’.			
CALM	0:	At least one measurement is running at the moment.			
	1:	TDC is calm: No measurement is running at the moment (default).			

**) PRE is stored in a separate register*

Table 6.1: Description of the Status Flags

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6.9 Daisy Chain Interface

The TDC provides a daisy chain interface for cascading of up to 31 TDC10000 in a chain. So it's possible to get very fast and efficiently access to the measurement results of all chips.

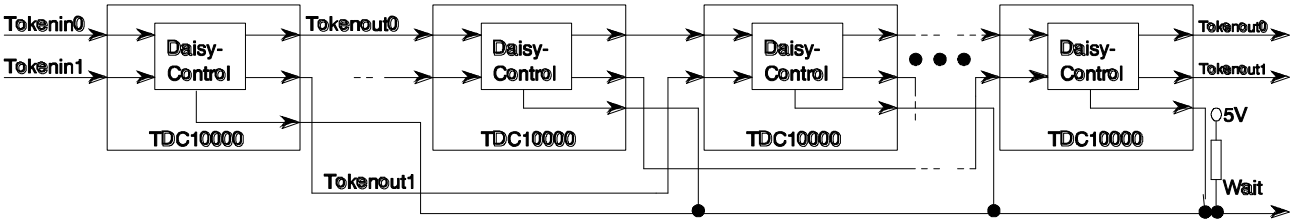

Figure 6.10 Daisy Chain Interface

The TDC10000 can be chained as represented in Figure 6.10 using the tokenin and tokenout pins. Since each TDC has two tokenin pins and two tokenout pins the chips can be cross connected in such a way that tokenout0 leads to the next chip and tokenout1 leads to the chip after next. With the possibility to select the output the token is passed on, chips which are not to be read out can be masked.

6.9.1 Daisy Chain Configuration Cycle and Chip Number Assignment

After power-on reset all chips have the default chip number 31. At the beginning of the daisy chain configuration cycle the global instruction WRDAISY is sent to all chips. Now all chips wait for the token and a simultaneous write strobe to store their daisy chain configuration and chip number. The token is sent to the first chip by setting one of the tokenin pins to '1'. With the rising edge of the following write strobe the 8 lower data bus lines are written into the register GLOBREG1. This register contains the information about the chip number, which token-output is used and how the chip will react when the chain is read out. A description of the individual bits of GLOBREG1 is to be found in Chapter 7.3.3, Global Register GLOBREG1. Then the token is passed on to the next chip.

This sequence is continued until the token drops out of the last chip in the chain. This event can be set up to interrupt the connected processor, which ends the configuration cycle by removing the token from the first chip.

After configuration each chip should have its unique chip number which will enable direct addressing. The chip numbers should be assigned in a descending order in which the chip number 0 has to be assigned to the last chip in the chain. If, for example, all possible 31 numbers are assigned, the chips should be numbered descending from 30 down to 0.

If the WAIT-outputs of the TDCs (pins WAIT) are used for the control of the connected processor, the last chip in the daisy chain has to be configured especially so that the processor doesn't remain in the Wait State after reading the last measurement result. Setting the bits LASTCHIP and TKSEL in the register GLOBREG1 to '1' will configure this chip to hold the WAIT-line at '0' after the last measurement result is read out. It has to be taken into account that in this configuration the token is supplied by the output TOKOUT1.

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6.9.2 Daisy Chain Read-Mode

The daisy chain is read out in a similar way as it is configured. After a measurement several chips have one or more valid measurement results ready for readout. Writing the global instruction DAIRDON, all TDCs are set to the daisy chain read-mode, available only in the 16-bit mode. In the daisy chain read-mode every chip waits for the token. The first chip selected to be read - which does not have to be the first chip of the daisy chain - receives the token from one of the tokenin pins or by the local software instruction SETTOKEN. If no measurement results are ready for readout the token is passed on to the next chip in the chain immediately with a delay of approx. 10ns (5V, typ). If the chip has valid measurement results for readout, the chip retains the token and its data are read out with every read strobe in the following order: First the measurement results of channel 0 are read - if there are any - then the measurement results of channel 1 and finally a special status word, if the special-daisy-read-mode is selected within the register GLOBREG1. When all available data is read the token is passed on to the next chip.

This sequence is continued until the token drops out of the last chip in the chain. This event can be used to signal the completion of the daisy-read sequence. The daisy chain read-mode is turned off by the global instruction DAIRDOFF and the token has either to be removed from the pin or reset by the local instruction RESTOKEN.

If a large number of consecutive chips in the daisy chain doesn't contain valid data, then the time between the readout of two chips having valid measurement results may be longer than the time between two read strobes of a fast processor.

If so, the WAIT-outputs of the TDCs can be used: All WAIT pins are driven by open drain buffers and have to be connected to a shared pull-up resistor. This WAIT-line can be connected to the WAIT-input of a processor. When the daisy chain read-mode is turned off, then the WAIT-line is drawn to '0'. When the daisy chain read-mode is turned on, then the WAIT-outputs of all chips are HiZ and the pull-up resistor pulls the WAIT-line to '1' as long as the token is not retained by a chip. This means, that during the time when the token is passed on and no valid data is available, the processor is kept in the Wait State until the token has come to a chip with valid data for readout. As mentioned before, the last chip has to operate in a special mode, drawing the WAIT-line to '0' when the token drops out of the last chip. Otherwise the processor would remain in the Wait State.

After turning on the daisy chain read-mode the WAIT-line remains '0' and isn't pulled up to '1' until the first rising edge of the read strobe. So if the WAIT-control is used for reading out the daisy chain the following steps are to be executed for each read-sequence:

1. Turn on the daisy chain read-mode.
2. Set the token via tokenin pin or by instruction.
3. Wait for 10ns * number of chips (5V, typ), so that the token has time to reach a chip with valid measurement results or to drop out of the last chip in the chain, if no valid results are available.
4. Read out the daisy chain until the token drops out of the last chip.
5. Turn off the daisy chain read-mode.
6. Remove token.

If the WAIT-control is not used the daisy chain read-mode may remain active and the token may be removed and set again before starting the next read-sequence.

6.9.3 Processorless Mode

For single chip applications the ‚Processorless Mode' is selectable by setting pin NOPROC to '1'. In this mode no configuration of the TDC is possible. All measurements are performed in measurement mode 0, the ‚Default Mode'. So before switching to the Processorless Mode be sure to execute a power-on reset guaranteeing the TDC to be in default state.

In the Processorless Mode there is no the need of any opcode or chip number and the TDC can be controlled using just simple logic: The measurement results can be read out using only the correct number of read-strobes according to the selected bus width. First the measurement results of channel 0 are read - if there are any - then the measurement results of channel 1. When the last result has been read, further read strobes will cause the measurement results to be read again, however this data will not be valid signified by the VALID-flags set to 0.

7 Programming of the TDC10000

All instructions written into the TDC's Instruction Register are decoded by the TDC. If meant for it, the instructions are executed.

7.1 Execution of Instructions

The following steps are necessary so that the TDC10000 executes an instruction:

At first the TDC must recognise that an instruction is meant for it. This is done by either addressing the chip directly or by selecting all chips connected to a bus.

The TDC is addressed directly by a ***local*** instruction that contains the *opcode* of the instruction and a *chip number* (see Figure 7.1). If this chip number corresponds to the chip number assigned to the TDC during the daisy chain configuration cycle, then the TDC executes the instruction. In 8-bit mode the chip number and the opcode are written separately (2 write cycles), in 16-bit mode writing an instruction takes only one cycle.

If an instruction is marked as ***global*** by setting the GLOBAL BIT (Bit5), then it is accepted by all TDCs.

16-bit Instruction (local and global *)

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
X	**X**	**X**	**CHIP NUMBER (31 - 0)**				
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
X	**X**	GLOBAL BIT	**OPCODE (31 - 0)**				

* When global 16-bit instruction the chip number doesn't care because all TDCs accept the instruction

8-bit Instruction (local and global **)

1.part 8-bit Instruction (CHIP NUMBER)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
X	**1**	**0**	**CHIP NUMBER (31 - 0)**				

2.part 8-bit Instruction (OPCODE)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
X	**0**	GLOBAL BIT	**OPCODE (31 - 0)**				

** When global 8-bit instruction the first part of the instruction (chip number) is not necessary, because all chips accept the instruction.

Figure 7.1: Format of Instructions

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There are instructions that are executed immediately after writing the instruction register (e.g. RESET, see Chapter 7.1.1) and there are instructions that expect further actions for completion. These actions can be write or read cycles. If, for example, a Mode Register is to be written then the TDC expects a further write strobe to store the new data provided on the data bus. In doing so the execution of the instruction is completed and after this the TDC accepts a new instruction. The same procedure applies to a read: The TDC, after decoding the opcode for reading e.g. the Status Register, expects a read strobe to put the contents of the Status Register on the bus.

In accordance with Figure 7.1 there are four types of instructions:

Local 8-bit instruction:

Writing a local 8-bit instruction into the TDC needs two write cycles:

1. Bit 6 of the first byte has to be set to '1' indicating the five lower bits to be the chip number. Bit 5 is set to '0'.
2. The five lower bits of the second byte contain the opcode of the instruction. The three upper bits should be set to '0'.

If the instruction is an instruction with three or more cycles, the corresponding number of read or write strobes has to follow.

Global 8-bit instruction:

Writing a global 8-bit instruction into the TDC needs only one write cycle: Bit 5 (GLOBAL BIT) is set to '1' and bit 6 is set to '0'. The five lower bits contain the opcode of the instruction. If the instruction is an instruction with two or more cycles, the corresponding number of read or write strobes has to follow.

Local 16-bit instruction:

One word is written into the TDC with bit 5 (GLOBAL BIT) set to '0'. Bits 12 - 8 contain the chip number, in the bits 4 - 0 the opcode of the instruction is stored. If the instruction is an instruction with two or more cycles, the corresponding number of read or write strobes has to follow.

Global 16-bit instruction:

One word is written into the TDC with bit 5 (GLOBAL BIT) set to '1'. Bits 4 - 0 contain the opcode of the instruction. All other bits doesn't care. If the instruction is an instruction with two or more cycles, the corresponding number of read or write strobes has to follow.

Important notes:

1. If several TDCs share a common bus a global read instruction may have fatal effects: If all TDC10000 connected to the common bus access at the same time bus conflicts will occur and the TDCs or other components may be corrupted. Therefore after power-on a daisy chain configuration cycle should be executed so that each chip gets its unique chip number (see Chapter 6.9.1). This chip number must not be 31: TDCs having a chip number different from 31 ignore global read accesses. After chip number assignment bus conflicts are impossible.
2. If a TDC10000 is operated as single chip, all instructions can be executed as global instructions, because no bus conflicts are possible. Global read instructions are only accepted if a TDC has the default chip number 31. Therefore a stand-alone TDC with the chip number left unchanged within the register GLOBREG1 after power-on will accept all global read instructions.

7.1.1 List of Instructions (Opcodes)

Opcode Name	OPCODE	Description	8-Bit Mode *)	16-Bit Mode
RESET	**0**	Software-Reset of all registers, except GLOBREG0/1	1/2 CYCLES	1 CYCLE
RESK0	**1**	Software-Reset of channel 0 and MODREG0	1/2 CYCLES	1 CYCLE
RESK1	**2**	Software-Reset of channel 1 and MODREG1	1/2 CYCLES	1 CYCLE
WRMREG0	**3**	Write MODREG0 channel 0	2/3 CYCLES	2 CYCLES
WRMREG1	**4**	Write MODREG1 channel 1	2/3 CYCLES	2 CYCLES
WRGREG0	**5**	Write GLOBREG0	2/3 CYCLES	2 CYCLES
WRGREG1	**6**	Write GLOBREG1	2/3 CYCLES	2 CYCLES
WROFF0	**7**	Write OFFSET0 channel 0	2/3 CYCLES	2 CYCLES
WROFF1	**8**	Write OFFSET1 channel 1	2/3 CYCLES	2 CYCLES
RDK0 **)	**9**	Read measurement results channel 0	4/5 CYCLES	2 CYCLES
RDK1 **)	**10**	Read measurement results channel 1	4/5 CYCLES	2 CYCLES
RDSTAT	**11**	Read Status Register	2/3 CYCLES	2 CYCLES
RDMREG0	**12**	Read MODREG0 channel 0	2/3 CYCLES	2 CYCLES
RDMREG1	**13**	Read MODREG1 channel 1	2/3 CYCLES	2 CYCLES
RDGREG0	**14**	Read GLOBREG0	2/3 CYCLES	2 CYCLES
RDGREG1	**15**	Read GLOBREG1	2/3 CYCLES	2 CYCLES
RDLOCK	**16**	Read multiplication factor of resolution-lock unit	2/3 CYCLES	2 CYCLES
RDK0M0	**17**	Read M0 channel 0	3/4 CYCLES	2 CYCLES
RDK1M0	**18**	Read M0 channel 1	3/4 CYCLES	2 CYCLES
WRLOCKMOD	**19**	Write register LOCKMOD of the resolution-lock unit	2/3 CYCLES	2 CYCLES
WRLOCK	**20**	Write external multipl.-factor of the resolution-lock unit	2/3 CYCLES	2 CYCLES
WRDAISY	**21**	Start daisy chain config. cycle + chip number assignment	2/3 CYCLES	2 CYCLES
SETTOKEN	**22**	Set token by software	--	1 CYCLE
DAIRDON	**23**	Turn on daisy chain read-mode	--	1 CYCLE
DAIRDOFF	**24**	Turn off daisy chain read-mode	--	1 CYCLE
RESTOKEN	**25**	Reset token set by software	--	1 CYCLE
EXOSZON	**26**	Enable calibration clock-input CALCLK	1/2 CYCLES	1 CYCLE
EXOSZOFF	**27**	Disable calibration clock-input CALCLK	1/2 CYCLES	1 CYCLE
HOLD	**28**	Switch resolution-lock unit to HOLD	1/2 CYCLES	1 CYCLE
TRACK	**29**	Switch resolution-lock unit to TRACK	1/2 CYCLES	1 CYCLE
INVALID	**30**	Invalid OPCODE -- no action --	--	--
COMABORT	**31**	Abort read instructions RDK0/1 (Opcode 9 + 10)	1/2 CYCLES	1 CYCLE

Notes:

*) 8-Bit Mode: First number is the number of cycles needed as global instruction, second number is the number of cycles needed as local instruction.

**) RDK0 and RDK1: Minimum number of cycles needed for these opcodes (see Chapter 7.1.2)

Table 7.1: List of Instructions (Opcodes)

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7.1.2 Description of the Instructions

RESET - Software-Reset: Resets the chip to its default state except of GLOBREG0, GLOBREG1 and the M0-Registers.

RESK0 - Software-Reset Channel 0: Resets Channel 0 and MODREG0 to the default state. Measurement results already stored in the Result-FIFO of channel 0 are not deleted.

RESK1 - Software-Reset Channel 1: Resets Channel 1 and MODREG1 to the default state. Measurement results already stored in the Result-FIFO of channel 1 are not deleted.

WRMREG0 - Writes Mode Register MODREG0 of channel 0.

WRMREG1 - Writes Mode Register MODREG1 of channel 1.

WRGREG0 - Writes Global Register GLOBREG0.

WRGREG1 - Writes Global Register GLOBREG0.

WROFF0 - Writes Offset Register OFFSET0 of channel 0.

WROFF1 - Writes Offset Register OFFSET1 of channel 1.

RDK0 - Reads the measurement results form channel 0. This read instruction is only activated if the FIFO of channel 0 has at least one valid measurement result for readout and the flag VALID0 is set to '1'. The instruction remains active until the last measurement result of channel 0 is read out and VALID0 is cleared to '0'. Now a new instruction is accepted by the TDC. If not all of the measurement results have to be read, the instruction can be aborted by the instruction COMABORT (Opcode31).

If not reading out a measurement result immediately after a measurement but waiting until another measurement is completed and stored in the Result-FIFO, then both results can be read without having to rewrite RDK0.

RDK1 - Reads the measurement results form channel 1. This read instruction is only activated if the FIFO of channel 1 has at least one valid measurement result for readout and the flag VALID1 is set to '1'. The instruction remains active until the last measurement result of channel 1 is read out and VALID1 is cleared to '0'. Now a new instruction is accepted by the TDC. If not all of the measurement results have to be read, the instruction can be aborted by the instruction COMABORT (Opcode31).

If not reading out a measurement result immediately after a measurement but waiting until another measurement is completed and stored in the Result-FIFO, then both results can be read without having to rewrite RDK1.

RDSTAT - Reads the Status Register.

RDMREG0 - Reads register MODREG0 of channel 0.

RDMREG1 - Reads register MODREG1 of channel 1.

RDGREG0 - Reads register GLOBREG0.

RDGREG1 - Reads register GLOBREG1.

RDLOCK - Reads the internal multiplication factor of the resolution-lock unit's Latch 8.

RDK0M0 - Reads the value of the characteristic quantity M0 of channel 0. If 16-fold accuracy is selected, this value is 16 times as large as with 1-fold accuracy.

RDK1M0 - Reads the value of the characteristic quantity M0 of channel 1. If 16-fold accuracy is selected, this value is 16 times as large as with 1-fold accuracy.

WRLOCKMOD - Writes the LOCKMOD-Register of the resolution-lock unit.

WRLOCK - Writes the external multiplication factor into the LOCKREG-Register of the resolution-lock unit.

WRDAISY - Starts the daisy chain configuration cycle and the chip number assignment.

SETTOKEN - Sets the token. This instruction must always be local. *)

RESTOKEN - Resets the token set by SETTOKEN (default). *)

DAIRDON – Turns on the daisy chain read-mode. *)

DAIRDOFF – Turns off the daisy chain read-mode (default). *)

EXOSZON - Enables the calibration clock-input CALCLK (default), if not disabled by pin ENOSZ.

EXOSZOFF - Disables the calibration clock-input CALCLK.

HOLD - Switches the resolution-lock unit to Hold-Mode.

TRACK - Switches the resolution-lock unit to Track-Mode (default).

INVALID - Invalid opcode, no operation is executed.

COMABORT - Aborts the read instructions RDK0 and RDK1 even when the corresponding FIFO isn't empty. If only a part of a measurement result is read (e.g. the fractional portion in the 16-bit mode) before COMABORT is executed then this part is read out later once again.

*) *Available only in 16-bit mode*

7.2 Read Registers and Data Format of Measurement Results

Readout data on 8-bit data bus

Data bits->	7	6	5	4	3	2	1	0
GLOBREG1	SDRSW	LASTCHIP	TKSEL	CHIP NUMBER 0 - 31				
GLOBREG0	RESLOCK	CALDIV	CALDIV0	INHM	DELAY	SPEED	16*M	AUTO_M0
MODREG0	NOISE	DIS_CHAN	STOP_INV	START_INV	RETRIGGER	M0_GEN	MESSMODE1	MESSMODE0
MODREG1	NOISE	DIS_CHAN	STOP_INV	START_INV	RETRIGGER	M0_GEN	MESSMODE1	MESSMODE0
STATUSREG	0	0	CALM	VALID1	VALID0	READY1	READY0	SYSERR
LOCKREG	MULTIPLICATION FACTOR OF RESOLUTION-LOCK UNIT BITS <7..0>							
1.VALUE *	FRACTIONAL PORTION BITS <13..6> (UPPER BITS)							
2.VALUE *	INTEGER PORTION BITS <7..0> (LOWER BITS)							
3.VALUE *	FRACTIONAL PORTION BITS <5..1> (LOWER BITS)					INT. PORTION BITS 9+8		CHANN. NUMBER
PRE (1.part)	PRECOUNTER BITS <7..0> (LOWER BITS)							
PRE (2.part)	0	0	0	0	PRECOUNTER BITS <11..8> (UPPER BITS)			
M0 (1.part)	M0 BITS <7..0> (LOWER BITS)							
M0 (2.part)	0	0	0	M0 BITS <12..8> (UPPER BITS)				

Readout data on 16-bit data bus

Daten Bits->	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GLOBREG1	SAME AS GLOBREG1 WITH 8-BIT								SAME AS GLOBREG0 WITH 8-BIT							
GLOBREG0	SAME AS GLOBREG1 WITH 8-BIT								SAME AS GLOBREG0 WITH 8-BIT							
MODREG0	SAME AS MODREG1 WITH 8-BIT								SAME AS MODREG0 WITH 8-BIT							
MODREG1	SAME AS MODREG1 WITH 8-BIT								SAME AS MODREG0 WITH 8-BIT							
STATUSREG	SAME AS LOCKREG WITH 8-BIT								SAME AS STATUSREG WITH 8-BIT							
LOCKREG	SAME AS LOCKREG WITH 8-BIT								SAME AS STATUSREG WITH 8-BIT							
1.VALUE *	0	CHAN.-NUMBER	FRACTIONAL PORTION BITS <13..0>													
2.VALUE *	0	CHIP NUMBER 0 - 31							INTEGER PORTION BITS <9..0>							
PRE	0	0	0	0	PRECOUNTER BITS <11..0>											
M0	0	0	0	M0 BITS <12..0>												
SDRSW	1	CHIP NUMBER 0 - 31							K1OV	K0OV	K1ME	K0ME	0	0	0	0

Note: * Measurement value or calibration value

Data format (measurement values / calibration values):

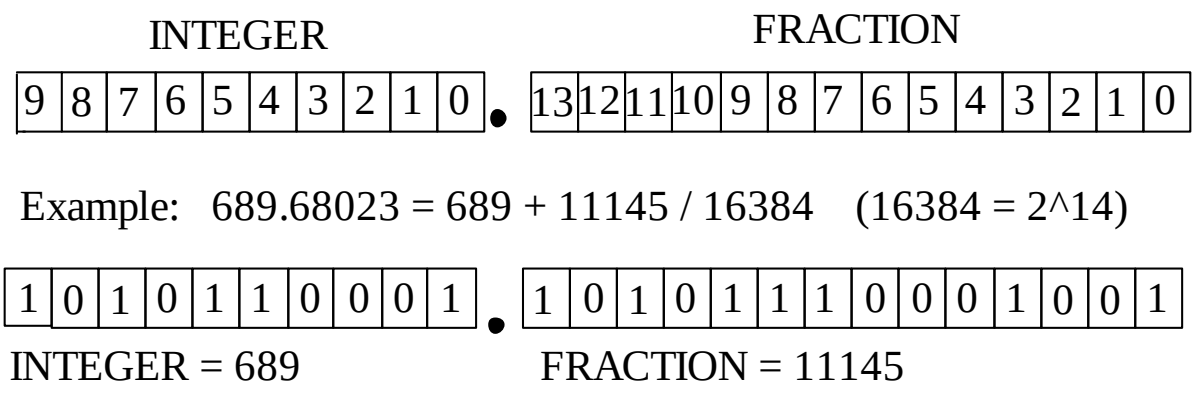

Figure 7.2: Read Registers and Data Format of Measurement Results

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7.3 Write Registers

The default value of all write registers is 0. The default chip number of the Global Register GLOBREG1 is 31. The only register having no default is the LOCKMOD Register. When writing new data into these registers in 16-bit mode be sure to provide them via data lines D[7..0] of the data bus.

7.3.1 Mode Registers MODREG0/1

Channel 0 is configurated by MODREG0, channel 1 is configurated by MODREG1. These registers are identical and independent of each other.

Bit1 and Bit0: MEASUREMENT MODE (MESSMODE1, MESSMODE0):

Binary coded measurement mode:

00: Measurement mode 0 (default) 10: Measurement mode 2
01: Measurement mode 1 11: Measurement mode 3

Bit2: SEPARATE M0-MEASUREMENT(M0_GEN):

Setting this bit to '1' generates a new characteristic quantity M0 for the respective channel no matter if the channel is disabled or not by software or pin. M0 is generated with 1-fold accuracy or 16-fold accuracy depending on the configuration and stored in the appropriate M0-Register. After completion of the separate M0-measurement this bit is cleared automatically. During the separate M0-measurement the channel is not ready for measurement.

Bit3: RETRIGGER-UNIT (RETRIGGER) **):

0: off (default)
1: on

Bit4: EDGE-SENSITIVITY START (START_INV) *):

0: Start-input triggers on rising edge (default)
1: Start-input triggers on falling edge

Bit5: EDGE-SENSITIVITY STOP (STOP_INV) *):

0: Stop-input triggers on rising edge (default)
1: Stop-input triggers on falling edge

Bit6: DISABLE KANAL (DIS_CHAN):

0: Measurement channel enabled, if pin ENA0 = 1 resp. ENA1 = 1 (default)
1: Measurement channel disabled

Bit7: AUTO NOISE UNIT (NOISE) ***):

0: off (default)
1: on

*) *Before changing the edge-sensitivity the respective channel has to be disabled via software or pin.*
**) *Bit relevant only for measurement modes 0 and 1. Have to be set to'0' for modes 2 and 3.*
***) *Bit relevant only for measurement modes 0 and 3. Have to be set to'0' for modes 1 and 2.*

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7.3.2 Global Register GLOBREG0

GLOBREG0 is for configurations concerning both channels.

Bit0: AUTOMATIC M0-MEASUREMENT (AUTO_M0):

0: on, if pin INHMD = 1 (default)
1: off

Bit1: M0-ACCURACY (16*M0):

0: M0-generation with 1-fold accuracy (default)
1: M0-generation with 16-fold accuracy

Bit2: ALU-SPEED (SPEED):

0: fast, if pin SPEED = 0 (default)
1: slow

Bit3: DELAY-LINES (DELAY):

0: off (default)
1: on

Bit4: MEAS/CALC-SUPPRESSION (INHM):

0: Simultaneous measurements and ALU-calculations allowed (default)
1: Either measurements or ALU-calculations

Bit6 and Bit5: CALIBRATION CLOCK DIVIDER (CALDIV1, CALDIV0):

00: 1:1 (default) 10: 1:8
01: 1:4 11: 1:16

Bit7: RESOLUTION-LOCK UNIT (RESLOCK):

0: off, if pin RLOCKON = 0 (default)
1: on

7.3.3 Global Register GLOBREG1

GLOBREG1 is the configuration register of the daisy chain interface.

Bit4 to Bit0: CHIPNUMBER:

After power-on reset the default chip number is 31. TDCs having this chip number accept all global instructions, even the read instructions. This is useful for single-chip applications, because no chip number has to be assigned when global instructions are used.

Bit5: TOKENOUT-SELECT (TKSEL):

This bit selects which output will pass on the token. Setting the bit to '0' selects TOKOUT0, setting the bit to '1' selects TOKOUT1.

Bit6: LASTCHIP *):

This bit acts in combination with the WAIT-line. If the daisy chain read-mode is controlled by the WAIT, this bit and bit5 (TKSEL) have to be set to '1' during the configuration of the last chip of the chain, so that the connected processor doesn't remain in the Wait State after all results are read out.

Bit7: SPECIAL-DAISY-READ-STATUS-WORD (SDRSW) *):

If this bit is set to '1', then during a daisy chain read-sequence a special status word (SDRSW) is read instead of measurement results from chips still running measurements or chips with the overflow bit set. This status word has its highest bit set to '1'.

**) Bit relevant only for 16-bit mode.*

7.3.4 Offset Registers OFFSET0/1

In these registers correction values are stored for ALU-calculations preventing the ALU to go into overflow when measuring very small time differences. A wrong value written into an offset register may cause the ALU to go ´Out of Range´. **Therefore it's highly recommended not to change the default value 0 of the offset registers.** If changing nevertheless, then the 8 bit value to be written is a two's complement. Values of +/-30 shouldn't be exceeded. If measurement errors of 10ns or more should occur during measurement, then please change the value of the respective Offset Register to smaller absolute values.

7.3.5 LOCKMOD Register

This register is the configuration register of the resolution-lock unit. It has no default settings. Therefore this register has to be initialised before activating the resolution-lock unit. When using a 4 MHz reference clock and the internal multiplication factor, 0 is recommended for initialisation.

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
x	x	x	x	x	x	0	internal multiplication factor is used
x	x	x	x	x	x	1	external multiplication factor is used
x	x	x	0	0	0	x	Reference clock divider 1:64 *)
x	x	x	0	0	1	x	Reference clock divider 1:128
x	x	x	0	1	0	x	Reference clock divider 1:256
x	x	x	0	1	1	x	Reference clock divider 1:512
x	x	x	1	0	0	x	Reference clock divider 1:1024 **)
x	x	x	1	0	1	x	Reference clock divider 1:2048
x	x	x	1	1	0	x	Reference clock divider 1:4096
x	x	x	1	1	1	x	Reference clock divider 1:8192
0	0	0	x	x	x	x	internal ringoscillator clock divider 1:16 *)
0	0	1	x	x	x	x	internal ringoscillator clock divider 1:32
0	1	0	x	x	x	x	internal ringoscillator clock divider 1:64
0	1	1	x	x	x	x	internal ringoscillator clock divider 1:128
1	0	0	x	x	x	x	internal ringoscillator clock divider 1:256 **)
1	0	1	x	x	x	x	internal ringoscillator clock divider 1:512
1	1	0	x	x	x	x	internal ringoscillator clock divider 1:1024
1	1	1	x	x	x	x	internal ringoscillator clock divider 1:2048

Note: If the clock dividers factors of reference clock and ring oscillator clock are identical (examples: *) and **)), then the reference clock is the ringoscillator clock divided by four.

Table 7.2: LOCKMOD Register of the Resolution-Lock Unit

Bit0 of LOCKREG selects whether the unit is to be operated with the internal or with the external multiplication factor. Bits 1, 2 and 3 adjust an additional division factor for the reference clock. Bits 4, 5 and 6 adjust an additional division factor for the internal ringoscillator clock. Bit 7 should be set to ‘0’ when initialising the register.

7.3.6 LOCKREG Register

If the resolution-lock unit is to be operated using an external multiplication factor, then this factor has to be written into the register LOCKREG as 8-bit UNSIGNED INTEGER value before switching to the external factor.

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8 Appendix

8.1 Electrical Specifications

8.1.1 Recommended Operating Conditions

Beyond these ranges a stable operation of the TDC10000 cannot be guaranteed.

Parameter	Symbol	Conditions	min	max	Unit
Supply Voltage	VDD		2.7	5.5	V
Input Signal Voltage	Vi		0	VDD	V
Ambient Temperature	Ta		-40	+85	°C
Input Voltage High TTL	VIH	4.5V ≤ VDD ≤ 5.5V	2.2	VDD	V
Input Voltage Low TTL	VIL	4.5V ≤ VDD ≤ 5.5V	0	0.8	V
Input Rise/Fall Time	tr, tf		0	200	ns

Table 8.1: Recommended Operating Conditions

8.1.2 Absolute Maximum Ratings

Operating the chip beyond these values could destroy the device immediately.

Parameter	Symbol	Conditions	Values	Unit
Supply Voltage	VDD		-0.5 ... +6.5	V
I/O Voltage	Vi/Vo		-0.5 .. VDD+0.5	V
Output Current	Io	IOL(min)=9.0 mA	20	mA
Operating Temperature	Topt		-40 .. +85	ºC
Storage Temperature	Tstg		-65 .. +150	ºC

Table 8.2: Absolute maximum Ratings

8.2 Accuracy of Measurement

8.2.1 Measurements in Measurement Mode 0 (Default Mode)

When measuring in measurement mode 0, immediately after time measurement a calibration measurement is executed. Caused by the preceding measurement the supply voltage of the TDC10000 is still unstable during generation of the first calibration value. If the calibration clock is generated using the on-chip oscillator (see standard wiring) the interference is passed to the oscillator, which reacts with higher jitter. Thus an additional error of up to several hundred picoseconds may be added to the result of the first calibration value. Therefore measurement mode 0 is not recommended for reaching the highest possible measurement accuracy when using the on-chip oscillator.

This effect can be reduced significantly when using an external calibration clock instead of the on-chip oscillator.

In this measurement mode measurements with a standard deviation of approx. 85ps in the single shot mode can be achieved.

8.2.2 Measuring with highest possible Accuracy

For getting the highest possible measurement accuracy the following proceeding is recommended:

Measurement mode 1 is used for time measurements. The calibration measurements are executed separately in regular intervals via measurement mode 2. In order to achieve high quality calibration values, averaged calibration values are used executing multiple calibration measurements within a calibration cycle. Averaging factors of 16 up to 32 have proved well in practice. In nearly all cases one calibration cycle per second is sufficient.

In this measurement mode measurements with a standard deviation of approx. 60ps in the single shot mode can be achieved.

8.3 Measurements with Resolution-Lock

If the measurement task does not allow the execution of regular calibration measurements, it is possible to operate the chip in the resolution-lock mode. In this case it is most favourable, to generate very exact calibration values by executing multiple calibration measurements while the chip operates in the resolution lock mode. Calibration values once generated, can be used further on and calibration measurements are needed no longer.

Please note that in spite of using resolution-lock the resolution can’t kept constant infinitely. Huge variations in temperature and long measurement times may cause deviations of up to several LSBs: A 50K change in temperature will cause an error of approx. 0.15% (0.003 %/K), for instance. That results in an error of 1,5 ns/µs measurement time.

Operating in the resolution-lock mode measurements with a standard deviation of approx. 60ps in the single shot mode can be achieved.

8.3.1 Example of Activating the Resolution-Lock Unit

In the following the operating sequence of activating the resolution-lock unit is shown in an example. Global instructions are used: The GLOBAL BIT is set (see Chapter 7.1, Execution of Instructions). In addition the internal multiplication factor is used as well as a 4 MHz reference clock:

1. Write LOCKMOD Register of the resolution-lock unit:

WRITE_TDC(51) /* global write (decimal) of register LOCKMOD (32 + 19) */
WRITE_TDC(0) /* value, that is stored in the register LOCKMOD */

2. Prepare Track-Mode:

TH (pin 14) to '0'
WRITE_TDC(61) /* switch to Track-Mode by software for safety's sake (32 + 29) */

3. Enable resolution-lock unit in the register GLOBREG0 (enable Track-Mode):

WRITE_TDC(37) /* opcode for writing to GLOBREG0 (32 + 5) */
WRITE_TDC(128) /* set bit 7 to '1', all other bits to '0' */

4. Switch to Hold-Mode:

Wait for a short time (e.g. 1 second and then switch TH (pin 14) to '1'. Now the control loop is closed. The pin PHASE (pin 7) indicates whether the PLL has locked or not. Here a clock with a pulse/mark-ratio of approx.1:1 should be generated. Cooling down the chip the 1-phase of the clock should be reduced visibly.

Important Note:

If the suggested analog external circuit with the LM7805 is used (see Figure 6.7), it is not recommended to use the software instruction to switch to the Hold-Mode, since the circuit will lock then hardly never.

8.4 Dead Times

The values shown in Table 8.3 are maximum times. The actual dead time of a measurement can be substantially shorter. It varies as a function of the measured time difference.

Measurement Cycle	Dead Time t_{dead}
Time measurement only	80ns < t_{dead} < 300ns
Time measurement with M0-generation 1-fold	150ns < t_{dead} < 400ns
Time measurement with M0-generation 16-fold	1200ns < t_{dead} < 3600ns
Time measurement with automatic calibration measurement and M0-generation 1-fold	400ns + 5 calibration clocks, minimum 1200ns
Time measurement with automatic calibration measurement and M0-generation 16-fold	3600ns + 5 calibration clocks, minimum 5000ns

Table 8.3: Dead Times (typical at 5V, 25°C)

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8.5 Behavior of the TDC at SYSERR

If the maximum measurement period of a measurement range is exceeded or the stop-signal is missing completely, the measurement channel overflows. The channel is disabled, the flag SYSERR is set to '1' and all further start- or stop-signals are ignored.

Resetting the channel clears this error condition and SYSERR is set to '0'. If the retrigger unit is enabled, also the next retriggering start-signal clears SYSERR to '0' and the measurement is restarted.

If an overflow has occurred and SYSERR is set to '1', then the Status Register may report, that only the flag SYSERR is set and no valid measurement results are ready for readout although this is not correct. There is a simple way to find out the truth:

Step 1: Software-Resets on both channels (Opcode 1 and 2). So the SYSERR is cleared, if it was caused by a channel's overflow. The measurement results stored in the Result-FIFOs are not deleted by this Software-Resets.

Step 2: Read out the Status Register once again to find out if there are valid measurement results for readout.

Step 3: If so, read out the results of the appropriate channel(s).

8.6 Power-On Characteristics

The minimum pulse width of a high active power-on reset pulse connected to pin PURES is 100µs. Figure 8.1 shows a possible reset circuit (RC-circuit).

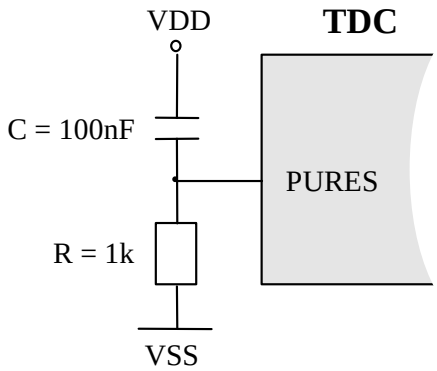

Figure 8.1: Reset Circuit

After a power-on reset the TDC is in the default state: Both channels are ready for measurement if they are not disabled by pin. Both channels are in measurement mode 0, the default mode.

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8.7 Application Notes

8.7.1 Standard Wiring of the TDC10000

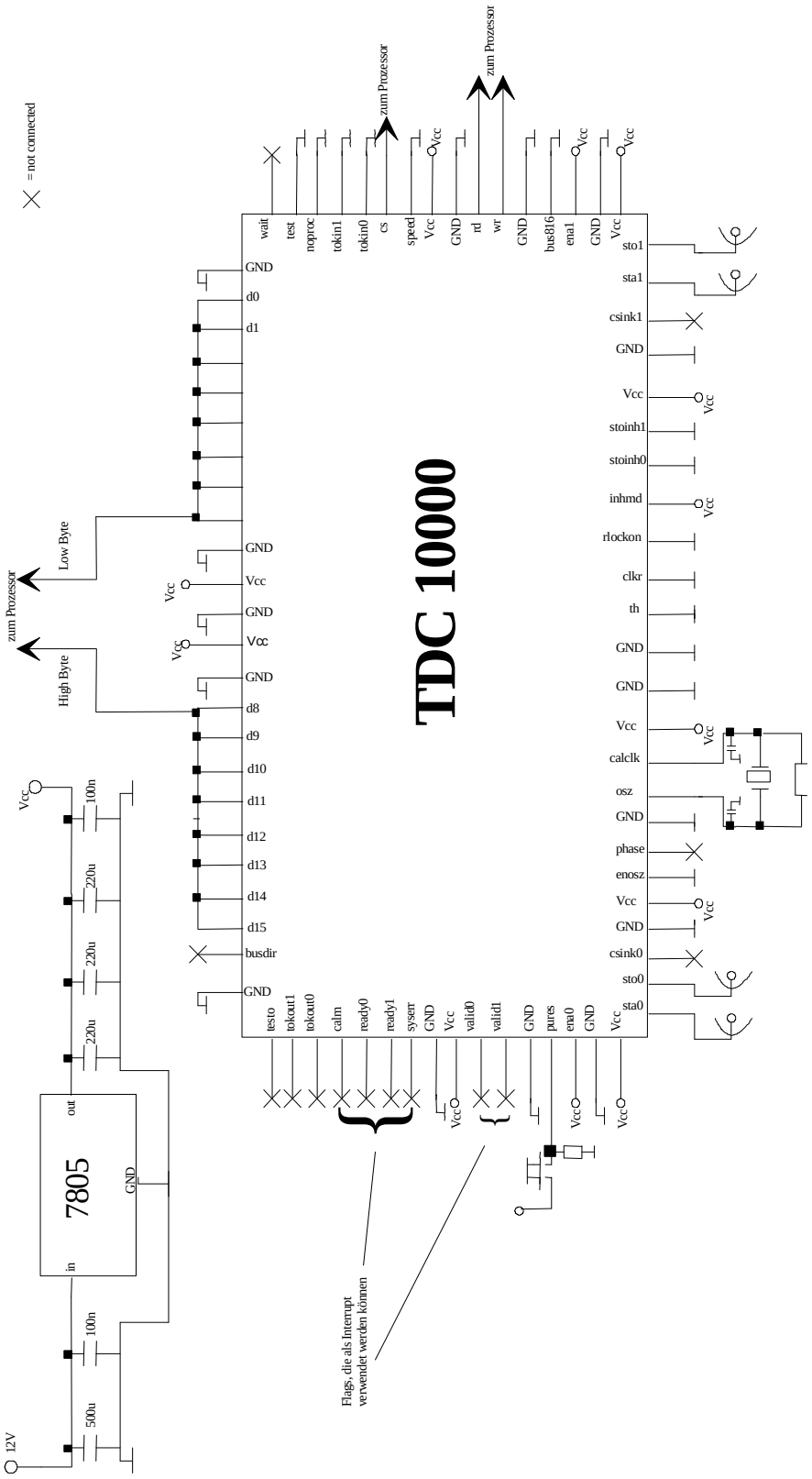

Figure 8.2: Standard Wiring of the TDC10000

8.7.2 Wiring for Measurement Mode 0

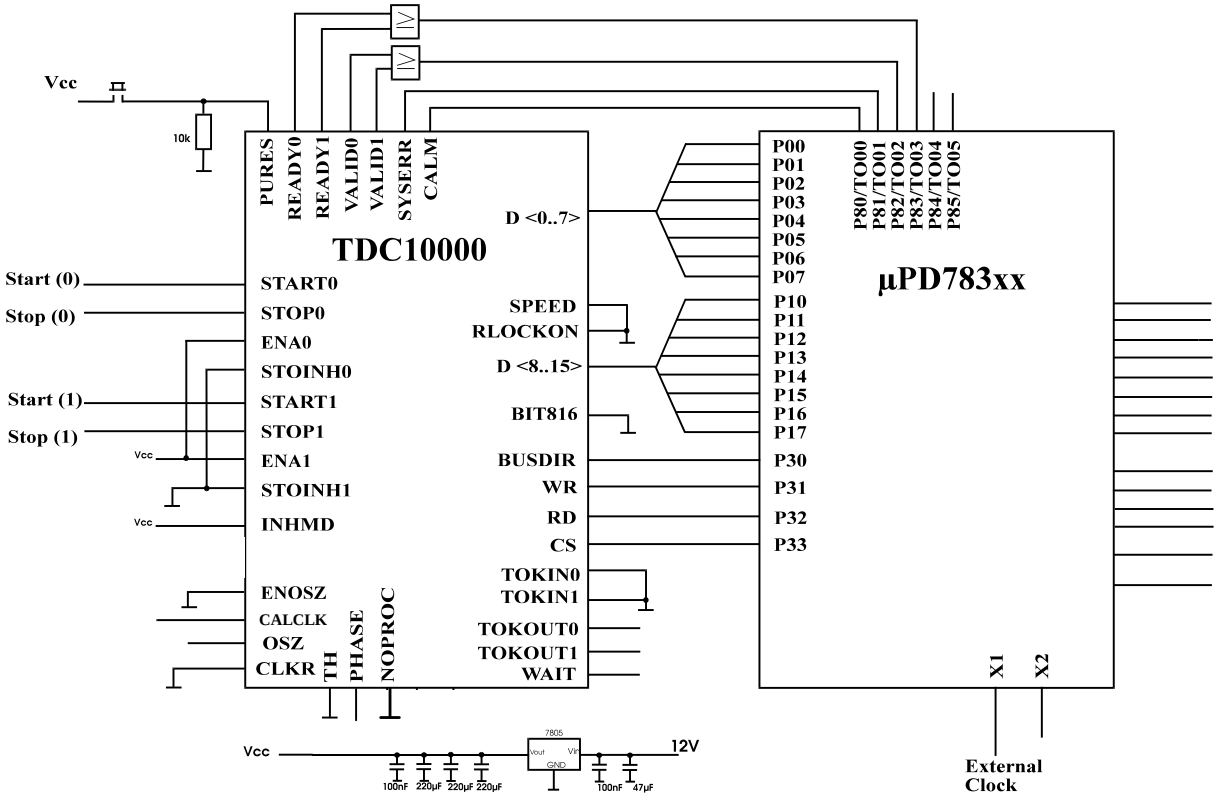

Figure 8.3: TDC10000 Single Chip with µPD783xx

Notes:

- 16 bit data bus for µPD78366.
- External calibration clock for the TDC10000.
- The resolution-lock unit cannot be used because there is no external PLL-wiring.
- All unused outputs should be left unconnected.

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8.7.3 Wiring for Measurement Mode 1

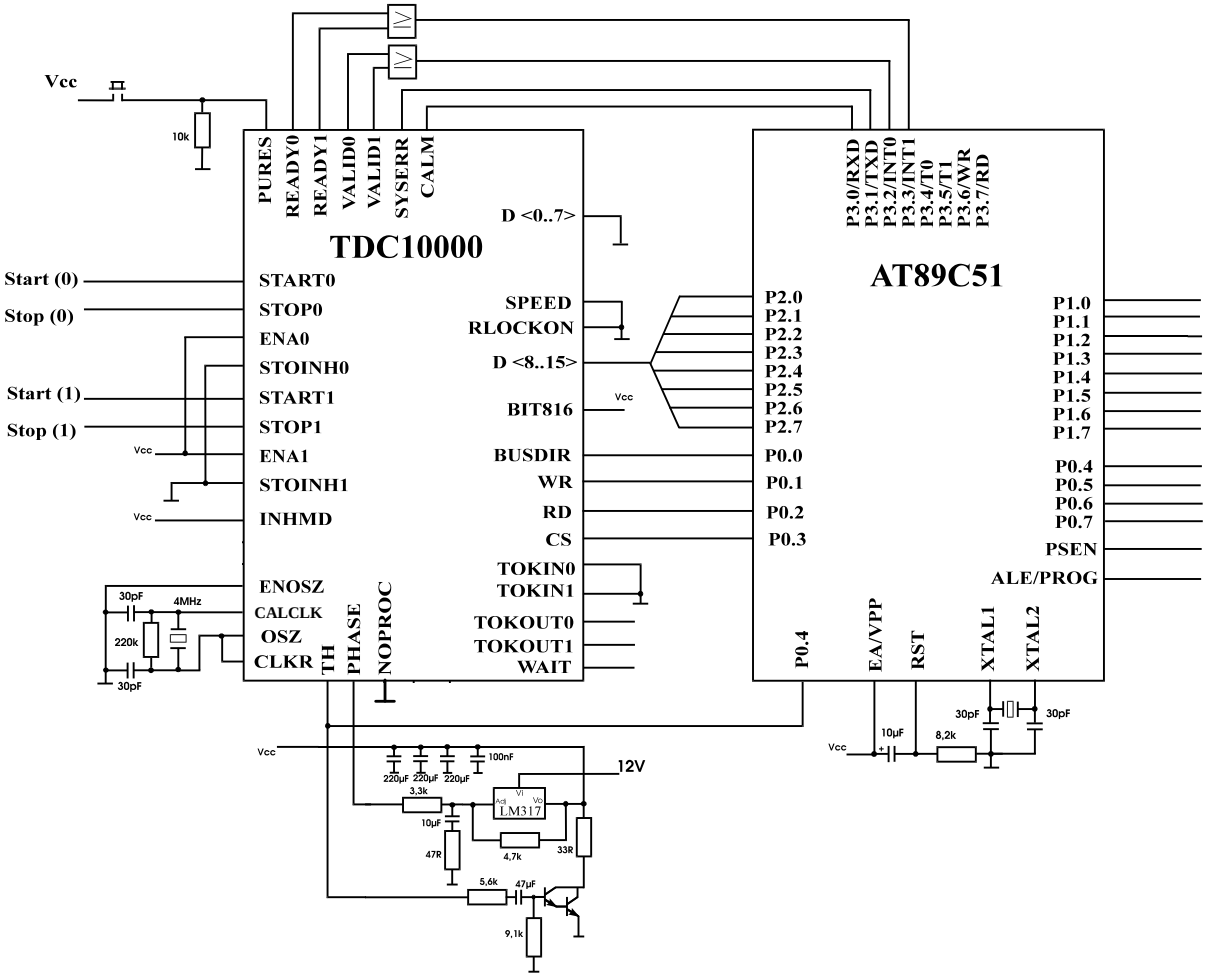

Figure 8.4: TDC10000 Single Chip with AT89C51

Notes:

- 8 bit data bus for AT89C51.
- External PLL-wiring.
- Resolution-lock unit activated by software.
- On-chip oscillator generates calibration clock.
- All unused outputs should be left unconnected.

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